Silicon Tunnel FETs for digital and analogue applications

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Kurzfassung

Aufgrund der steigenden Zahl von Transistoren pro Einheitsfläche in integrierten Schaltungen erlangt die Verlustleistung zunehmende Bedeutung. Die Verringerung der Versorgungsspanung VDD ist eine wichtige Maßnahme die dynamische und statische Leistungsaufnahme zu reduzieren. Aufgrund der inhärenten physikalischen Begrenzungen eines Metal-Oxide-Halbleiter-Feldeffekttransistors (MOSFET), führt dies zu entweder einem reduzierten An-Strom Ion oder erhöhtem Aus-Strom Ioff. Der Tunnel-Feldeffekttransistor (TFET) hingegen ist ein vielversprechendes Bauelement, welches erlaubt diese Begrenzungen zu überschreiten. Dies ist möglich, da der TFET auf quantenmechanischen Band-zu-Band Tunneln als Hauptladungstransport beruht, im Vergleich zur thermischen Emission bei MOSFETs.

In dieser Arbeit werden zwei verschiedene Vorschläge eines TFET-Konzeptes diskutiert, die auf Punkt- und Linien-Tunneln basieren. Beide Konzepte sind jeweils hinsichtlich Band-zu-Band Tunnelns optimiert, auf Basis physikalischer Modelle, welche sich aus der WKB-Näherung ergeben. Die Optimierung diente dem Ziel, einen höheren An-Strom und bessere inverse Unterschwellensteigung SS (<60 mV/dec) zu ermöglichen. Die auf Punkt-Tunneln basierenden TFETs verwenden einen einzelnen Nanodraht (NW), der auf verspannten Silizium-auf-Isolator (sSOI) prozessiert wird. Der Nanodraht ist rundherum von einem High-k/Metal-Gate umgeben, um die elektrostatische Kontrolle des Kanals zu optimieren. Ionenimplantation und Aktivierung von Dotierstoffen wurden sorgfältig angepasst, um die Qualität des Tunnelkontaktes Schritt für Schritt zu verbessern. Der optimierte TFET zeigt verbesserten An-Strom Ion, Ion/Ioff Verhältnis sowie sehr gutes mittlere SSavg. Zusätzlich werden verschiedene Analog-Eigenschaften der Nanodraht TFETs präsentiert. Tieftemperaturmessungen ermöglichen eine Verschlechterung der Leistung von NW-TFETs bei kleinen Gatespannungen nachzuweisen, welche Tunneln über Störstellen (TAT) entstammt

Um ungewolltes ambipolares Verhalten zu verhindern, welches in jedem TFET inhärent auftritt, wird ein TFET mit einem SiO2 Abstandhalter im Drain-Gate Zwischenraum vorgestellt. Dies unterdrückt effektiv den Tunnelkontakt auf der Drain-Seite. Als Folge wird das ambipolare Schaltverhalten vollkommen unterdrückt, wodurch die Eignung der TFETs sowohl im Bereich digitaler als auch analoger Anwendungen gezeigt wird.

Als zweites Konzept wird ein planarer Si TFET hergestellt, der auf Linien-Tunneln basiert, welches bessere Unterschwell-Eigenschaften ermöglicht. Nach Ionenimplantation und Aktivieren der Dotierstoffe wird der Source-Schicht verdünnt, so dass Implantationsschäden entfernt werden. Die so gefertigten Bauelemente zeigen sehr deutlich verbesserte SS von 55 mV/dec über zwei Dekaden des elektrischen Source-Drain-Stroms.

Inverter Schaltungen aus komplementären NW-TFETs (CTFETs), sowohl mit als auch ohne ambipolare Eigenschaften, wurden hergestellt und verglichen. Es konnte gezeigt werden, dass die Unterdrückung des ambipolaren Verhaltens den Rauschpegel positiv beeinflusst.

Eine hohe Temperaturstabilität von Stromspiegeln wird diskutiert, welche auf zwei NW-TFETs basieren. Die Messungen zeigen stabilen Betrieb der Schaltung auch bei hohen Temperaturen, wenn die Transistoren BTBT-Bereich arbeiten.

Abstract

As number of transistors per unit area in integrated circuits increases, power dissipation of the chips becomes progressively important. Scaling of supply voltage VDD is an important measure to decrease dynamic Pdynamic and static Pstatic power consumption of integrated circuits. However, considering inherent limitation of MOSFETs, this either leads to low operating current or increased leakage current. The tunnel field effect transistor (TFET) is a promising alternative to go beyond this limitation to operate devices at very small supply voltage VDD due to non-thermal quantum mechanical band to band tunneling as the main carrier transport mechanism compared to thermal emission in MOSFETs.

In this work, two different TFET design concepts based on point-tunneling and line-tunneling are investigated. In each case, the tunneling probability is optimized with regard to basic physical relations derived from the WKB approximation of band to band tunneling. The end goals are to achieve higher drive currents at lower supply voltages and subthermal (<60 mV/dec) inverse subthreshold swings. The point-tunneling based devices are fabricated as single nanowire gate-all-around TFETs based on tensile-strained silicon on insulator(sSOI) wafers. The devices are highly scaled and employ high-k HfO2 gate dielectric to achieve optimum electrostatic control over the channel. Moreover, careful adjustments of ion implantation and dopant activation in various settings ensure favorable tunneling junction formation. The optimized device shows superior on-current Ion, Ion/Ioff ratio as well very good average subthreshold swing SSavg. For this device, various analog figures of merits are also presented. Low temperature measurements reveal insights about the limiting effect of trap-assisted-tunneling(TAT) at low gate voltages on performance of the fabricated nanowire TFETs.

Parasitic ambipolar behavior which is inherent to TFET operation is suppressed by employing a SiO2 spacer to form a gate-drain underlap, effectively switching off the drain tunneling junction. As a result, the ambipolar behavior of NW TFETs fabricated by this method is completely suppressed, making them suitable for different digital and analog circuit applications.

To achieve enhanced subthreshold characteristics, line-tunneling based planar silicon TFETs are designed and fabricated by thinning down the source after implantation and dopant activation to get rid of the end of the range (EOR) damage. Devices

fabricated by this method show superior SS of 55mV/dec over two decades of drain current.

Complementary single NW TFET inverters with and without ambipolarity are fabricated and compared. It is revealed that the suppression of ambipolarity has a positive effect on noise margin of inverters, where the logic levels match the actual bias points.

High temperature stability of two-transistor current mirrors based on nanowire TFETs is also evaluated. The measurements show stable operation of the circuit even at high temperatures when the transistors operate in the BTBT region.

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Chapter 1

Introduction

According to CISCO's Global Cloud Index(GCI), by 2020 there will be more people with mobile phones than people who have access to conventional electricity distribution at home. Moreover, large scale use of sensors for internet of things(IOT) applications is booming and finding new applications in industry[1]. When billions of sensors are used, their size and power efficiency will be the most important issues[2]. Up to now, the semiconductor industry has managed to follow the Moore's law over 50 years by employing innovative designs like multi-gate transistors [3] or developing high-k dielectrics[4], and scaling down the technology node. Using high resolution deep ultraviolet light lithography techniques coupled with a gate-all-around device architecture, IBM fabricated 5nm silicon chips in 2017. Samsung plans to produce 4nm node chips by 2020. However, it may not be possible to continue this trend as leakage currents due to extreme physical limits will keep increasing[5]. Even though there has been immense technology leaps, Moore's law is slowing down, for example by 2013 Intel had already slowed down launching new technology nodes. As our society immensely relies on faster devices with lower power consumption, there is a need for new device concepts beyond the Moore's era.

As gate length of devices is reduced and number of transistors in an integrated circuit increases, the power dissipation caused by static and dynamic power consumption of the chips also increases dramatically. This is caused by the inherent physical limitation of MOSFET current in subthreshold region that can be increased with respect to gate voltage ideally with a rate of 60mV/dec at room temperature. The implication of this limit for power dissipation is two fold. Firstly, by decreasing V_{th} to scale downV_{DD}, I_{off} due to the 60mV/dec limit increases exponentially, causing static power consumption to rise. On the other hand, dynamic power consumption is dependent on the square of voltage bias, and thus by keeping the V_{th} constant and directly decreasing V_{DD}, dynamic power consumption can be greatly decreased. On

the other hand, this also hinders the switching frequency of the device, which is not desirable. New device concepts to achieve SS less than 60mV/dec are required to tackle this problem . Different field controlled switching mechanisms like mechanical switches[6, 7], impact ionization[8, 9], ferroelectricity[10] and band to band tunneling(BTBT)[11] can fulfill the SS requirement. In the current work we will focus on BTBT switching in tunneling field effect transistor(TFET) since it does not have limited switching speed associated with the other aforementioned mechanisms[12].

The earliest observation of band to band tunneling dates back to 1952 when Stuetze[13] recorded the ambipolar nature of a gated Ge p-n diode. Following that, in 1958 Esaki[14] discovered p-n interband tunneling. Over the years different TFET concepts were developed but it was not until 2004 when Appenzeller[15], Wang[16] and Bhuwalka[17] reported sub 60mV/dec switching in a TFET. Since then TFETs based on different materials like Si[18, 19, 20],Ge[21] and III-V materials[22] have shown sub 60mV/dec behavior, yet the average subthreshold slope for these devices is well above 60mV/dec and they also exhibit either low I_{on} current or low $I_{on}/\ I_{off}$ ratio. Among different materials, silicon based TFETs attract a lot of interest due to their compatibility with the conventional CMOS fabrication process and better material quality which helps to keep the costs low and makes it feasible to achieve complementary TFET circuits[23, 24].

Within the framework of this thesis, two different design concepts of TFETs will be evaluated. First, highly scaled silicon single nanowire TFETs with superior electrostatics and optimized doping processes for both n- and p- TFETs which are investigated for low-power analogue and digital circuit applications. Secondly, planar silicon TFETs with a novel approach to reduces trap assisted tunneling and exploit sharper switching of line tunneling are fabricated and also simulated by use of TCAD technology.

The content of this thesis is divided into five chapters. Following this introduction, the basic motivation, theory and concepts which are required to understand underlying physics are discussed in Chapter 2. Design considerations and non-ideal processes which limit performance of TFETs are specifically explained. Chapter 3 presents the experimental results of silicon single GAA nanowire TFETs and the course of carefully optimizing key-process parameters to achieve maximum I_{on} and minimum average subthreshold slope. In addition, analogue figures of merit, low temperature measurements and density of interface trap are also discussed. Last but not least,

systematic suppression of ambipolar behavior is also investigated. Next, chapter 4 presents the experimental results of fabricated complementary TFET logic inverter circuits. The TFET circuits have been fabricated with and without ambipolarity to compare the results. Moreover, high-temperature behavior of the inverter is also characterized. In Chapter 5 fabrication of a novel structure for taking advantage of line-tunneling in silicon TFETs is presented with experimental electrical characterization. It is shown that these devices can achieve average SS of 55mV/dec for low currents. Using TCAD simulation, the device working principles are inferred and explained in detail. Finally, in Chapter 6 results for experimental demonstration of a two-TFET current mirror are presented. It is shown that this circuit may operate stable even at elevated temperatures.

Chapter 2

Theoretical Background

This chapter begins by introducing the limitation of power supply scaling in conventional MOSFET technology and explaining how it motivates development of novel device structures like TFETs. Moreover, the working principle of MOSFET and TFET is, from physics point of view, discussed and compared. Subsequently, various design aspects as well as different non-idealities that pose significant challenges to TFET operation are explained.

2.1 Limitations of power scaling in ICs

In order to gain a deeper understanding how MOSFET inherently limits the supply voltage V_{DD} scaling at a given technology node, one should consider the power dissipation of its operation. It comprises of two distinct terms, namely dynamic and static power consumption, related to V_{DD}. It can be written as:

$$P_{Total} = P_{Dynamic} + P_{Static} = C_T.{V_{DD}}^2.f + V_{DD}.I_{off} \tag{2.1}$$

where C_T is the total capacitance when transistor switches, f is the switching frequency, I_{off} is the off-state leakage current.

Looking at this equation, it makes sense to decrease V_{DD} in order to scale down power dissipation. To achieve this goal, there are two options available: firstly to function in the subthreshold region by decreasing V_{DD} and keeping threshold voltage V_{th} unchanged(Figure 2.1(a)). This is not an ideal case because the operation frequency subsequently decreases.

The other measure to take is to scale down threshold voltage V_{th} in order to keep the on current high by lowering V_{DD}. This method, however, does not maintain a proper I_{on}/I_{off} ratio. To understand this issue one should understand the concept

of inverse subthreshold swing, abbreviated as SS. It basically quantifies the required voltage to increase current for an order of magnitude. This value for a MOSFET is physically limited to 60mV/dec at room temperature due to thermionic processes. Therefore, decreasing V_{th} is like shifting the whole $\log(I_d)$-V_{gs} curve to the left, hence increasing off-current exponentially, leading to much higher static power consumption(Figure 2.1(b)).

Considering this discussion, a novel device concept, like TFETs, is needed to overcome the 60mV/dec limit of MOSFETs as shown in Figure 2.1(a).

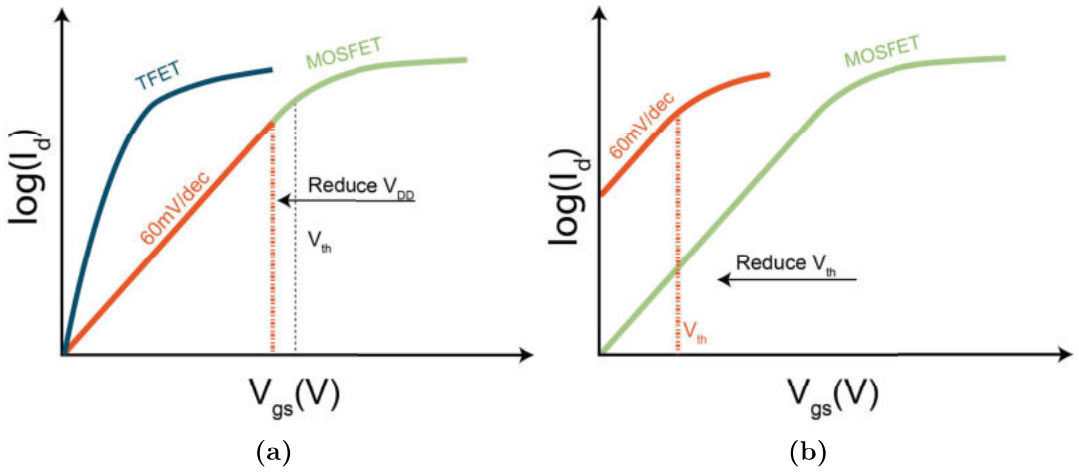


Figure 2.1: (a) Scaling down V_{DD} . In comparison the characteristics of a TFET is also depicted (b) Decreasing V_{th} to reach desired on current at a lower V_{DD}, resulting in high I_{off}.

2.2 MOSFET operation

Generally, field effect transistors (FETs) are semiconductor devices with two ohmic contacts, called drain and source, where charge transport between the two is controlled via a third one called the gate contact. The gate-channel structure is a metal-oxide-semiconductor (MOS) where the gate is separated by an insulating dielectric layer from the channel. An inversion layer beneath the oxide would act as a conducting channel where the carriers in case of a p-type substrate are electrons and in case of an n-type substrate are holes. The former case is called an n-MOSFET where the

latter is a p-MOSFET. Figure 2.2 shows the schematics and energy band diagram for an n-MOSFET at low and high V_{ds} voltages.

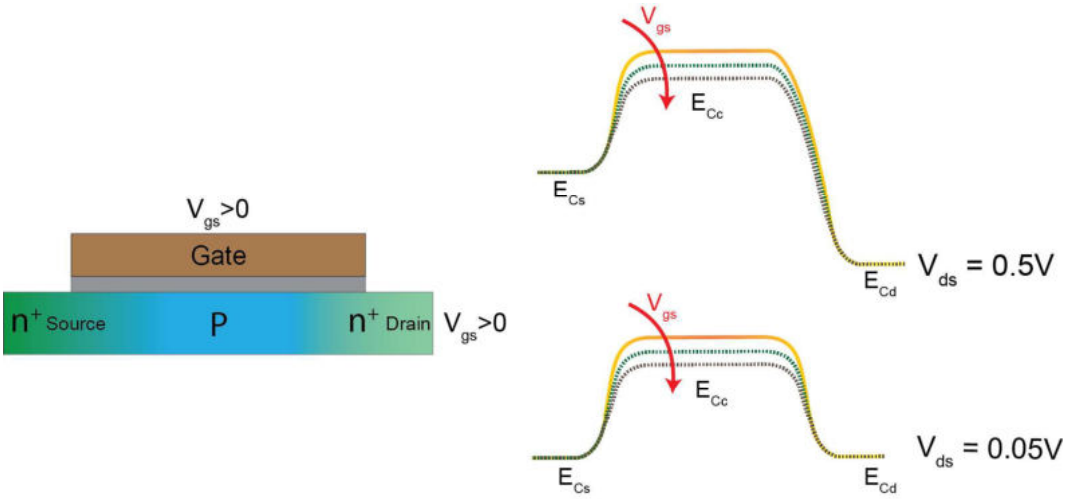


Figure 2.2: Schematic illustration of an n-MOSFET and its energy band diagram. By increasing the applied gate voltage V_{gs}, potential barrier height for electrons decreases allowing thermionic transport from the source to drain.

By moving the channel bands down, the thermally excited electrons can transmit from source to drain. To understand the physical limit of 60mV/dec for SS at room temperature, Landauer formalism can be used for the 1D case to evaluate the subthreshold behavior of MOSFET as follows:

$$I_d = \int_{-\infty}^{\infty} \frac{2e}{h} T(E)(f_s(E) - f_d(E))dE \tag{2.2}$$

where f_s and f_d are the Fermi distribution in source and drain, e is the elementary charge and h is the Planck constant. T(E) is the transmission probability from the potential barrier. For simplicity we let T(E) = 1 for energies higher than E > ${\phi_f}^0$ and otherwise T(E) = 0. ${\phi_f}^0$ denotes the conduction band energy of channel which is the potential barrier height for electrons. Therefore one can rewrite the relationship as:

$$I_d = \int_{{\phi_f}^0}^{\infty} \frac{2e}{h} (f_s(E) - f_d(E))dE \tag{2.3}$$

Since in the subthreshold region ${\phi_f}^0$ is much larger than the chemical potential of source μ_s and drain μ_d, f_s and f_d can be approximated by the Boltzmann distribution. Moreover, considering small V_{ds} voltage, then $f_s \gg f_d$ and one can approximate the previous equation as:

$$I_d = \int_{{\phi_f}^0}^{\infty} \frac{2e}{h} \exp\left\{\frac{\mu_s - E}{k_B T}\right\} dE = \frac{2e}{h} k_B T \exp\left\{\frac{\mu_s - {\phi_f}^0}{k_B T}\right\} \tag{2.4}$$

In order to calculate inverse subthreshold slope, we must rewrite I_d as a function of gate voltage V_g. The potential barrier height for carriers ${\phi_f}^0$ is dependent on the gate voltage through a capacitive voltage divider between gate oxide C_{ox}, interface capacitance C_{it} and depletion capacitance C_{dep}:

$$\frac{\partial {\phi_f}^0}{\partial V_g} = e \frac{C_{ox}}{C_{ox} + C_{it} + C_{dep}} \tag{2.5}$$

by inserting 2.5 into 2.4 inverse subtreshold slope SS can be calculated as follows:

$$SS = [\frac{\partial log I_D}{\partial V_g}]^{-1} = ln(10) \frac{k_B T}{e} (1 + \frac{C_{dep} + C_{it}}{C_{ox}}) \tag{2.6}$$

If the oxide capacitance is sufficiently large to reach the quantum capacitance limit($C_{dep} + C_{it} < C_{ox}$), then at room temperature T = 300K equ. 2.7 yields:

$$SS = ln(10) \frac{k_B T}{e} \approx 60 mV/dec \tag{2.7}$$

Therefore an ideal MOSFET in 1D structure with quantum capacitance limit will need a minimum of 60mV of gate voltage at room temperature to increase drain current by an order of magnitude.

2.3 Tunnel FET operation

A promising candidate to replace MOSFET in next generation low-power digital and analogue circuits is tunnel field effect transistor(TFET). It is basically a reversed biased and gated p-i-n diode as shown in Figure 2.3. The oppositely doped source and drain yields a staircase-like energy band structure for a TFET as shown in Figure 2.4. Depending on how the device is biased it may either function as an nTFET or a pTFET.

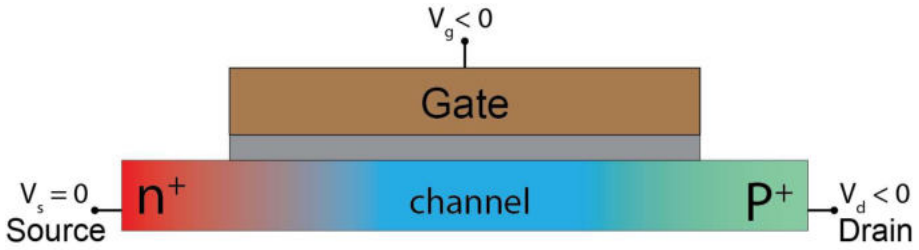


Figure 2.3: Schematic illustration of a TFET structure. It is a gated pin diode which is reversely biased through the gate on top of the gate oxide.

Here we assume a negative voltage V_d is applied on the p^+ doped junction and the n^+ doped junction is connected to the ground (Figure 2.3). As shown in Figure 2.4, firstly the device is in equilibrium and does not conduct current. By applying a negative voltage to the gate $V_{gs} < 0$, the energy bands in channel move up, and as soon as the valence band of channel E_{CV} moves above the conduction band of source E_{CS} an energy overlap window appears that allows carriers to tunnel from the source conduction band to the channel valence band, the distance of which, depends on the band-bending sharpness at the source-channel junction. This process is the so-called band to band tunneling (BTBT). In Figure 2.4 the energy overlap is marked as $\Delta\Phi$. Since tunneling of carriers outside of the energy overlap $\Delta\Phi$ is blocked, BTBT acts as a band-pass filter, filtering out the high and low parts of the Fermi distribution leading to smaller SS than 60mV/dec and less temperature susceptibility.

2.3.1 BTBT model

The band bending overlap at the source-channel junction of a TFET can be approximated as a triangular barrier as shown in Figure 2.5. Therefore, the tunneling probability T may be calculated using Wentzel-Kramers-Brillouin(WKB) approximation[25]:

$$T_{WKB} = -2\exp\left\{\int_{t_1}^{t_2} |k(t)|dt\right\} \tag{2.8}$$

where t_1 to t_2 is the tunneling path and k(t) is the wave vector of the carriers which for an electron with energy E in the conduction band E_C is given by:

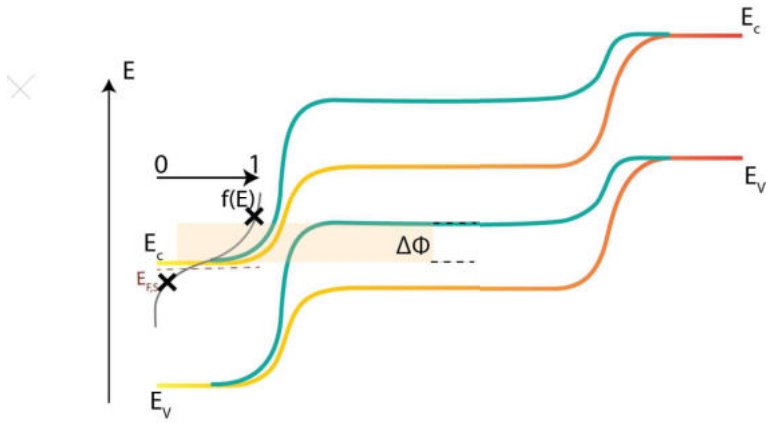


Figure 2.4: Illustration of TFET band structure when biased as a p-TFET. By increasing the absolute value of gate voltage V_g the channel bands move up until an energy overlap for BTBT between channel valance band and source conduction band appear.

$$k(t) = \sqrt{\frac{2m^*}{\hbar^2}(E - E_C)} = \sqrt{\frac{2m^*}{\hbar^2}(-e\xi t)} \tag{2.9}$$

Taking the integral after inserting 2.9 in 2.8 provides:

$$T_{WKB} = \exp\left\{-\frac{4\sqrt{2m^* {E_g}^{1.5}}}{3\hbar(e\xi)}\right\} \tag{2.10}$$

where ξ is the electric field being dependent on the band bending abruptness, which itself is a sum of doping and electrostatic screening lengths. Hence ξ can be approximated as $(E_g + \Delta\phi)/(\lambda_{ch} + \lambda_{dop})$, yielding from equ. 2.10:

$$T_{WKB} = \exp\left\{-\frac{4(\lambda_{dop} + \lambda_{ch})\sqrt{2m^* {E_g}^{1.5}}}{3\hbar(\Delta\phi + E_g)}\right\} \tag{2.11}$$

According to equ. 2.11 to achieve an optimum tunneling probability small E_g, small effective mass m^*, good electrostatics and sharp doping profile are needed.

2.3.2 TFET subthreshold behavior

Similar to a MOSFET, 1D Landauer formalism can be used to characterize subthreshold behavior of a TFET. For energies inside the band overlap $\Delta\phi$ carrier tunneling

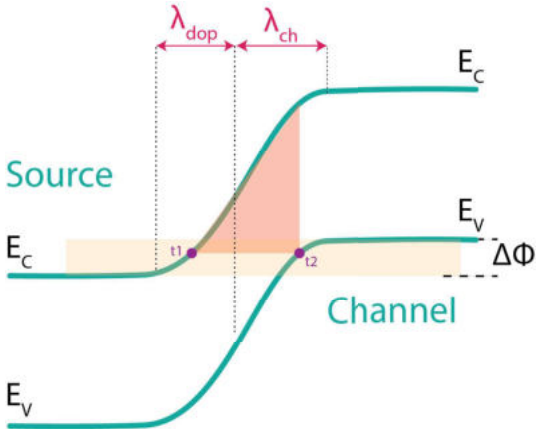


Figure 2.5: BTBT barrier in 1D is approximated by a rectangular shape.

probability T_{WKB} can be used, independent of energy E within the overlap interval, and otherwise equal to zero. Moreover, like MOSFETs, for small V_{ds} we can neglect carrier injection from drain. Therefore, the drain current I_D can be derived as:

$$I_d = \int_0^{\Delta\phi} \frac{2e}{h} T_{WKB} f_s(E) dE = T_{WKB} \frac{2e}{h} F(\Delta\phi) \tag{2.12}$$

where $F(\Delta\phi)$ is the Fermi–Dirac integral function. Now in order to calculate SS we should be able to calculate the partial derivative $\frac{\partial I_d}{\partial V_g}$. By assuming that our device has reached quantum capacitance limit where channel potential changes one by one with applied gate bias $e\frac{\partial V_g}{\partial \Delta\phi} = 1$, the partial derivative becomes:

$$\frac{\partial I_d}{\partial V_g} = e\frac{\partial I_d}{\partial \Delta\phi} = \frac{2e^2}{h}[\frac{\partial T_{WKB}}{\partial \Delta\phi} F(\Delta\phi) + T_{WKB}\frac{F(\Delta\phi)}{\Delta\phi}] \tag{2.13}$$

since it was assumed that T_{WKB} varies only slightly with energy E in the overlap region, therefore the first partial derivative in 2.13 can be neglected. Hence for small values of $\Delta\phi$ we may write:

$$SS = [\frac{\partial log I_D}{\partial V_g}]^{-1} = ln(10)[e\frac{\partial I_d}{\partial \Delta\phi}\frac{1}{I_d}]^{-1} = \frac{ln(10)}{e}\frac{F(\Delta\phi)}{\frac{\partial F(\Delta\phi)}{\partial \Delta\phi}} \approx \frac{ln(10)}{e}\Delta\phi \tag{2.14}$$

The derived relation shows that in contrast to MOSFETs, SS has no temperature dependence. However, SS changes by increasing gate voltage and may not be constant.

This happens because the tunneling current is dominated by the minimum tunneling distance due to the non-ideal band bending at the source.

2.3.3 Point tunneling vs line tunneling

In the previous section 2.3.1 the studied BTBT occurs immediately under the gate in the source-channel interface. Since this process takes place in a small area it is called point tunneling. However, if part of the gate overlaps the source, BTBT can also take place in the overlap region are perpendicular to the gate, which is called line tunneling. Figure 2.6 schematically depicts both of these BTBT processes. Since line-tunneling current has different gate voltage dependency than point-tunneling[26], its SS behavior can also be different. Line tunneling drain current can be written as[27]:

$$I_d \propto \sqrt{V_g - V_{onset}} \exp\{V_g - V_{onset}\} \tag{2.15}$$

where V_{onset} is defined as the required voltage to create the depletion region directly under the gate for line tunneling to kick in. By taking partial derivative of equation 2.15 and expanding it for small values of V_g:

$$SS = [\frac{\partial log I_d}{\partial V_g}]^{-1} \propto \sqrt{V_g - V_{onset}} = V_{onset} + \mathcal{O}(V_g) \tag{2.16}$$

Based on relation 2.16, SS associated with line tunneling in contrast to point tunneling has a smaller dependency on gate voltage, and may be considered constant for a small gate bias. However, it is worth noting that in a real device both processes are present but can be minimized or maximized by special device designs.

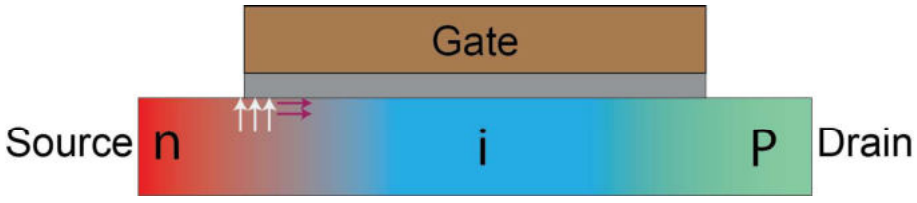


Figure 2.6: Schematic illustration of point and line tunneling processes. Point tunneling(violet arrows) is confined to a small area directly under the gate while line tunneling(white arrows) takes place along the gate-source overlap perpendicular to the gate. In a real device both of these tunneling mechanisms are more or less present.

2.4 TFET design factors

2.4.1 Electrostatic control

Gate structure

When calculating the tunneling probability T_{WKB} at Section 2.3.1, we found out that it has an exponential dependence on electrostatic screening length λ_{ch}. Thus it is imperative to minimize this value by providing higher electrostatic control over the channel. Solving the Poisson equation for SOI MOSFET devices on various gate structures has shown that by increasing the gate number on the channel, the screening length decreases [3, 28, 29]. Figure 2.7 schematically shows 3D representation of different gate structures. By solving the Poisson equations analytically for these well-defined gate structures the screening length can be calculated [30, 31, 32]:

$$\lambda_{Single-gate} = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{si} t_{ox}} \tag{2.17}$$

$$\lambda_{Double-gate} = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{si} t_{ox}} \tag{2.18}$$

$$\lambda_{GAA-Square} \approx \sqrt{\frac{\epsilon_{si}}{4\epsilon_{ox}} t_{si} t_{ox}} \tag{2.19}$$

$$\lambda_{GAA-Circular} = \sqrt{\frac{2\epsilon_{si} {t_{si}}^2 ln(1 + \frac{2t_{ox}}{t_{si}})}{16\epsilon_{ox}}} \tag{2.20}$$

where ϵ_{si}, ϵ_{ox} are the dielectric constant and t_{si} and t_{ox} are layer thickness for the silicon and oxide layer, respectively. For the sake of visualizing the impact of each gate structure, λ_{ch} values for the specified structures has been calculated in Figure 2.8 as a function of silicon layer thickness. Respective values for gate dielectric were taken 3nm HfO_2 with $\epsilon_{ox} \approx 18$ to match the main oxide layer used in this work. Compared to other gate structures, GAA achieves the best electrostatics, since it has the minimum λ_{ch}. For example, with silicon layer thickness of 5nm, the tunneling probability T_{WKB} for GAA structure is almost 5 times greater as the probability for planar structure. One downside to multi-gate device structure is having higher fabrication complexity, which translates to higher costs and lower production yield.

To indicate the effect of Si thickness on performance of a TFET, dc transfer

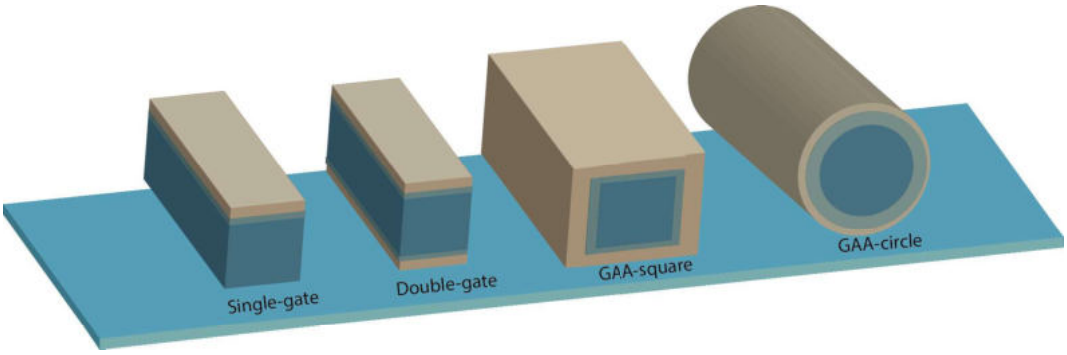


Figure 2.7: Schematics of different single and multi-gate structures. As number of gates increases, the complexity of fabrication also increases.

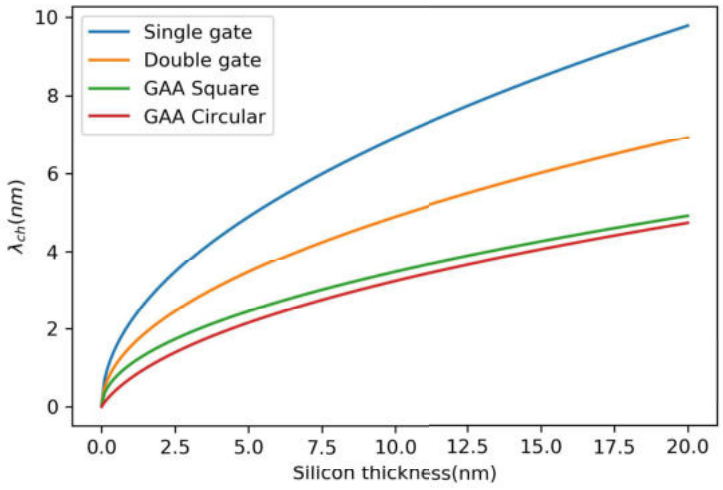


Figure 2.8: Calculation of screening length λ_{ch} for single and multi-gate device structures. The circular GAA structure achieves the best(the minimum) value of the parameter.

characteristics for a double-gate device with different channel thicknesses is simulated and shown in Figure 2.9. By decreasing the layer thickness, I_{on} and SS improve owing to a lower value for λ_{ch}.

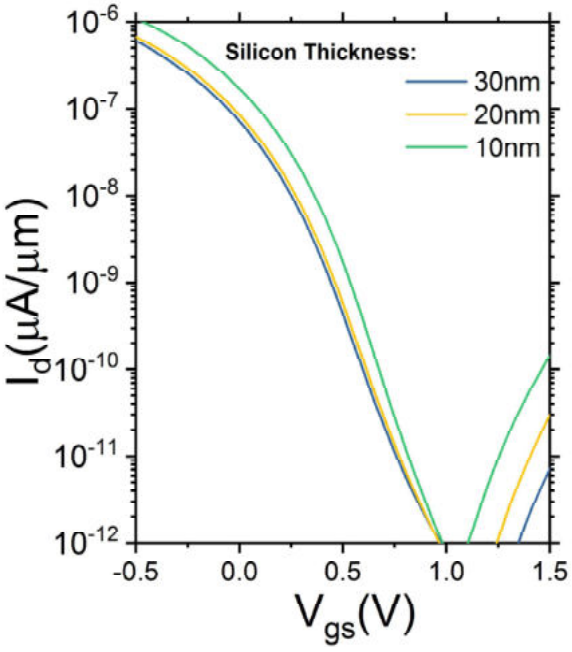


Figure 2.9: Simulated transfer characteristics of double gate TFETs for different Si thicknesses. I_{on} and average SS improve by decreasing the layer body-thickness.

Gate dielectric

Another important factor to achieve high electrostatic control over the channel, is optimizing gate oxide capacitance C_{ox}. In its simplest form the oxide capacitance features a double plate capacitor. The oxide capacitance for a GAA-square structure in strong inversion is calculated as [33]:

$$C_{ox_{GAA-square}} = \frac{2\pi\epsilon_{ox}}{ln(1+\frac{\pi t_{ox}}{2W})} \tag{2.21}$$

where W is the gate width on each side of the square. Looking at the equation, one method to increase capacitance is to increase W. However, this would be a bad choice since the actual capacitor will have a larger area leading to degradation of charging speed and scaling problems. By decreasing t_{ox} the oxide capacitance increases considerably which is favorable. Before 2007, the conventional CMOS technology used

SiO_2 as the gate oxide, due to its easy fabrication. However, by scaling SiO_2 down to small layer thickness $\approx 1.4nm$, the gate leakage current due to quantum tunneling of charge carriers through the thin oxide barrier increased aggressively, severely deteriorating device performance. Dielectric materials with higher permittivity than SiO_2 (the so-called high k dielectrics) have helped to solve this issue by providing the same oxide capacitance with a thicker layer. The most common of these high-k materials is HfO_2 with a permittivity of around $\epsilon_{HfO_2} \approx 20$ as compared to $\epsilon_{SiO_2} = 4.2$ for SiO_2. Many high-k materials like Al_2O_3, $ZrSiO_4$ and $LaLuO_3$ have been studied [34]. In order to have a standard scheme to easily compare these high-k materials, the equivalent oxide thickness(EOT) is defined as:

$$EOT = \frac{\epsilon_{SiO_2}}{\epsilon_{high-k}} d_{high-k} \tag{2.22}$$

where equation 2.22 basically converts the high-k material thickness into the equivalent SiO_2 thickness required to achieve the same oxide capacitance C_{ox}. In this work we deposit 3nm HfO_2 using atomica layer deposition (ALD) which translated into EOT = 0.66nm. However since there is about 1nm interfacial SiO_2 layer at the interface[35], the total EOT of the oxide capacitance is about 1.6nm.

Interface traps

Presence of traps in the silicon/oxide interface can lead to degraded electrostatics by screening the gate voltage control over the surface potential Φ^0. Ultimate negative effect of interface traps leads to Fermi level pinning [36], completely cutting off surface potential Φ^0 movements. Comprehensive surface cleaning prior to the gate stack deposition commonly decreases the number of such traps. In Chapter 3, the density of interface states D_{it} for a NW TFET has been measured using charge pumping method.

2.4.2 Doping profile

According to the tunneling probability relation T_{WKB}, λ_{dop} should be minimized to achieve higher BTBT currents. In this work we employ the concept of dopant segregation at $NiSi_2$/silicon interface as a means to achieve sharp doping profiles. This idea has been already thoroughly studied[37, 38, 39]. In this concept, firstly high-quality, single crystalline, low-resistivity $NiSi_2$ using a thin layer of Ni by annealing in

forming gas environment is formed. Next, carefully optimized implantation process is carried out in a way to restrain ions in the $NiSi_2$ layer. This prevents unnecessary damage to the silicon layer. Subsequently, a low-temperature annealing step drives the dopants out considering low solubility of dopants within the silicide forming a sharp doping profile with high concentration[40] by dopant segregation. G.V.Luong[41] has shown that this method enables doping profile of 4.1nm/dec for phosphorous in comparison to the conventional doping process which achieves a much broader doping profile of 8.7nm/dec.

2.5 TFET non-ideal processes

TFETs can theoretically surpass MOSFET performance at low supply voltages by achieving SS values smaller than 60mV/dec at room temperature. However, there are some non-ideal processes than deteriorating the TFET behavior, by masking the steepest part of SS or by parasitic conduction, particularly detrimental for circuit operation. In this section we will explore these non-ideal processes which negatively affect TFET performance and ways to amend them.

2.5.1 Trap assisted recombination

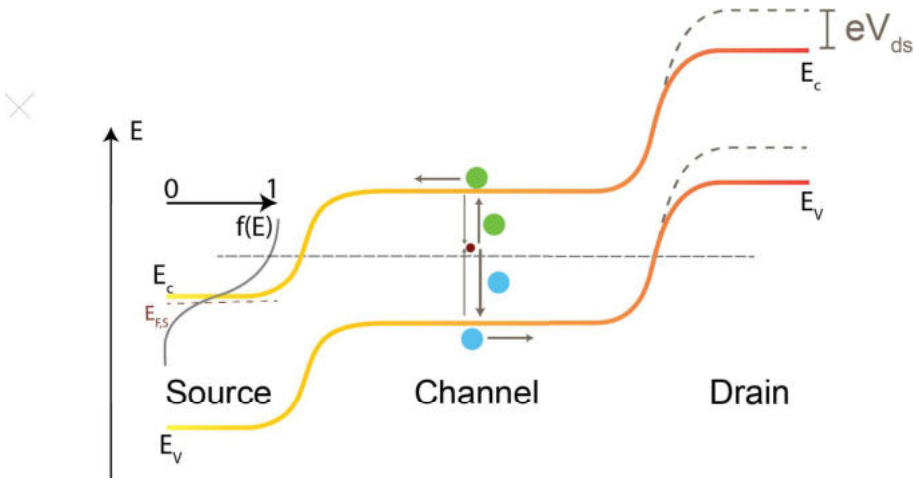


Figure 2.10: Illustration of trap assisted recombination within the bandgap of a TFET at off-state.

Trap assisted recombination or also commonly called Shockley-Read-Hall (SRH) recombination is the recombination and generation of carriers through deep level traps, induced for example by doping atoms impurity, located near the center of the semiconductor bandgap[42]. Since these traps assist carrier recombination/generation with the difference in the momentum, SRH is an important process in indirect semiconductors as silicon. In case of a reversely biased pin diode like TFET, SRH generation of current can be detected in the depletion region. Before applying a gate voltage, trap assissted tunneling (TAT) and BTBT do not contribute to the current and SRH mechanism is the main contributing factor to the off-state current of a TFET under flat-band conditions. The net recombination rate $\mathfrak{R}_{trap}$ for trap-assisted recombination by assuming zero field for a single trap is given as[43]:

$$\mathfrak{R}_{trap} = \frac{np - {n_i}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.23}$$

where n_i is the intrinsic and (p, τ_p) and (n, τ_n) are the hole and electron concentrations and carrier lifetimes, respectively. n_1 and p_1 are given by:

$$n_1 = n_i \exp\left\{\frac{E_T - E_F}{k_B T}\right\} \tag{2.24}$$

$$\mathrm{p}_1 = n_i \exp\left\{\frac{E_F - E_T}{k_B T}\right\} \tag{2.25}$$

where E_F is the Fermi energy and E_T is the energy of trap levels. When the p-i-n structure of TFET is reversed biased, the n and p concentrations in the depletion regions fall below that of n_i making the recombination rate $\mathfrak{R}_{trap}$ negative, meaning that carrier generation is larger than carrier recombination at zero field, before TAT and BTBT starts. Figure 2.10 schematically illustrates the SRH process in the bandgap.

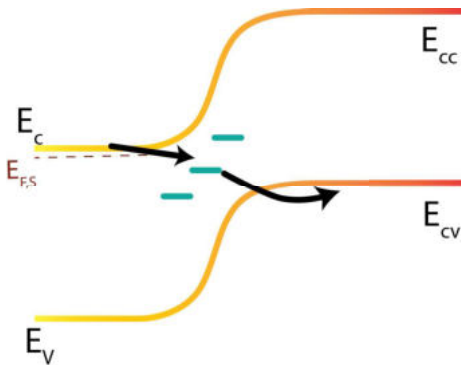


Figure 2.11: Schematics of trap assisted tunneling(TAT) process. Carriers tunneling into the available traps states at source/channel interface before being thermionically excited into the channel.

2.5.2 Trap assisted tunneling(TAT)

The oxide interface traps or the silicon defects in channel-source interface within the channel band gap induce trap assisted tunneling(TAT) by which the charge carriers can tunnel into the trap states and then reach the channel by thermal excitation, as indicated in Figure 2.11. It has been shown that TAT dominates at lower V_g voltages when an energy overlap for BTBT has not yet been created[44]. Since carriers get excited into the channel thermionically from the trap states, TAT depends on thermal broadening of the Fermi distribution function, making the resulting current limited to 60mV/dec at room temperature. Moreover, TAT masks the steepest region of TFET SS, severely deteriorating its performance. Figure 2.11 schematically depicts the process.

Since TAT is temperature dependent, it can be suppressed by cooling down the device, as shown in Chapter 3. Moreover, a study carried out in [45] confirms that by signaling the gate with short voltage pulses, TAT can be suppressed.

Hurkx et al[46] derived an expression for TAT by modifying the classical SRH equation with two field function factors Γ_n and Γ_p which account for tunneling from traps to the channel and taking its integral at a given position in pn junction depletion region:

$$\mathfrak{R}^{\mathrm{n}} = \int \frac{np - {n_i}^2}{\tau_p(\frac{n+n_1}{1+\Gamma_p}) + \tau_n(\frac{p+p_1}{1+\Gamma_n})} D_{it} dE \tag{2.26}$$

where $\mathfrak{R}^n$ is calculated per unit area and D_{it} is the interface trap density. According to 2.26, TAT generation rate is increases with n_i. This means that it is temperature dependent and increases with rising temperature and also with decreasing bandgap E_g . This indicates a trade-off for TFET design, since decreasing the bandgap to achieve better BTBT probability also amplifies TAT .

2.5.3 Super-linear onset

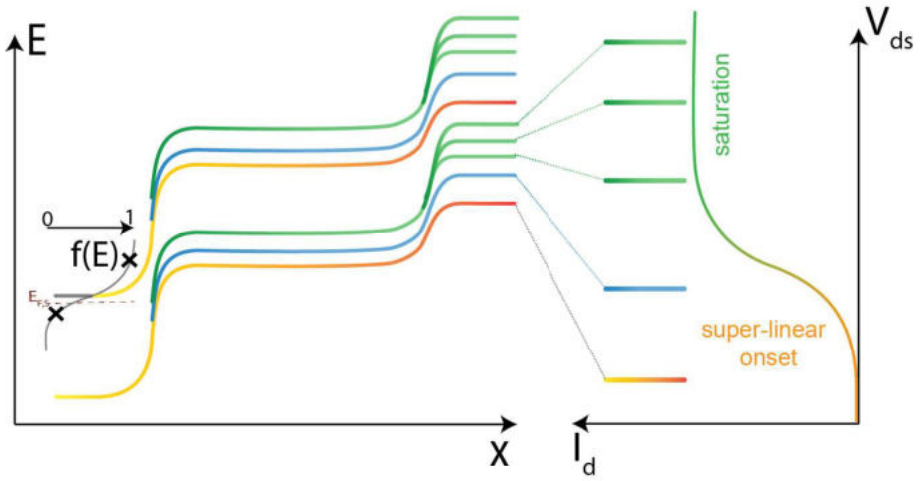


Figure 2.12: Schematic illustration of super-linear onset in a TFET output characteristics at sufficiently large gate voltage V_{gs}.

The output characteristics I_d-V_{ds} of a TFET can show exponential or the so-called super-linear onset as compared to the MOSFET. By applying a large enough gate voltage V_{gs} at small V_{ds}, the carriers generated by BTBT form an inversion charge Q_{inv} that screens the gate voltage. By increasing V_{ds}, Q_{inv} decreases and hence gate voltage screening is reduced. Consequently, channel bands move further reducing tunneling distance at source. This gives rise to the variable tunneling distance by changing V_{ds}. This process is called drain induced barrier thinning (DIBL) which is schematically shown in Figure 2.12. The super-linear onset can make different complications for analogue and digital circuit operation. For example, in case of a logic inverter, it can severely decrease the noise margin. Moreover, it negatively affects the intrinsic voltage gain A_{V_i}, an important analogue figure of merit.

Super-linear onset can be avoided by getting to the quantum capacitance limit(Cox » Cq), where surface potential changes one to one with gate voltage $\frac{\partial \phi_0}{\partial V_g} = 1$. However, quantum capacitance depends the on density of states(DOS), therefore this limit can be reached for the 1D device structures where the DOS has relates to the inverse square root of energy E. An example of such a device is GAA TFET with highly scaled silicon nanowire. Moreover, it has been shown in [47] that super-linear onset can be avoided by increasing the source doping concentration which extends the tunneling probability over a larger range of energies, thus limiting current discrepancy by varying V_{ds}.

2.5.4 Ambipolar behavior

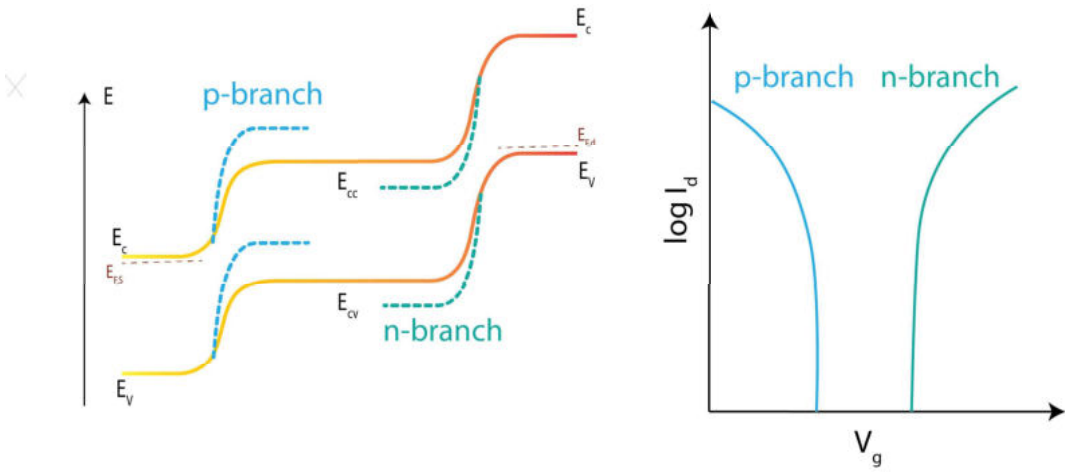


Figure 2.13: Schematic illustration of ambipolar behavior in a TFET.

Considering the symmetric structure of TFET, band to band tunneling may take place on both, source-channel and drain-channel junctions. As shown in Figure 2.13, depending on the gate voltage, bands in the channel can either move up or down, creating an energy overlap either in the source or in the drain junction. This behavior is the so-called ambipolarity, causing TFETs to conduct current for both positive and negative gate voltages. The separation of ambipolar branches depend on E_g and the applied V_{ds}, where it decreases by lowering E_g or increasing V_{ds}[48].

Ambipolar behavior is not desirable for proper function of TFET and therefore must be suppressed. As discussed above, the separation of ambipolar branches de-

pends on the drain voltage. For large enough V_{ds} voltages they can overlap and lead to higher I_{off} current. In other words, the off-current may not be dominated by thermionic leakage but BTBT from the drain side. Moreover, the ambipolarity can lead to circuit failure and malfunction. For example, in case of a C-TFET inverter, the logic levels may not match to the actual bias voltages. Thus when considering proper operation for circuits, ambipolar behavior must be eliminated. This can be achieved via creating a gate-drain underlap, reducing drain doping or using hetero-junction structures.

Chapter 3

GAA Single NW Silicon TFETs, experiment and simulation

3.1 Introduction

In this chapter seeks we investigate the effect of different process parameters on the performance of silicon NW TFETs. Silicon NW TFETs have already been fabricated in the past, but they were fabricated as an array of several NWs[23, 49, 24]. Due to the inherently high sensitivity of TFETs to process variations, it is challenging to optimize these devices by changing process parameters, since the outcome is an average of the characteristics of all of the NWs in the array. Therefore, we have evaluated TFETs comprising of only one single NW. We will begin this chapter by describing the fabrication process of nanowire TFETs then we will simulate and compare the effect of geometry variation on TFET performance with experimental results. Consequently, optimization of DC characteristics of NW TFETs by changing different process parameters will be discussed. Furthermore, trap assisted tunneling, as an important limitation on steep subthreshold slope SS is studied via different techniques. Lastly, systematic suppression of ambipolarity is demonstrated.

3.2 Device Fabrication

Substrate

To fabricate the devices strained silicon(sSi) on insulator (sSOI) with 15nm silicon and 145nm buried oxide was used as the starting substrate. sSOI wafers are fabricated by growing a strained silicon layer on relaxed SiGe and transferring it via bonding into a substrate with SiO_2 and silicon stack[50]. The substrates were supplied by Soitec SA and had a background doping of p = 1x10^{16} cm^{-3}. The strained SOI has a

biaxial stress of $\epsilon = 0.8\%$

Fabrication Process

The following presents the important fabrication steps for the gate all around device. Figure 3.1 schematically depicts the important fabrication steps.

- The sSOI wafers were covered by AZ resist and then cut into 20mmx20mm pieces. Then the AZ resist was striped away by acetone/propanol solutions. Any residues of the resist was removed in a barrel reactor by O_2 plasma(Figure 3.1(a)).

- E-beam markers were patterned and etched into the substrate to a depth of 700nm. Firstly, UV6.06 photo-resist was coated and marker patterns were transferred via optical lithography onto the samples. Secondly, the markers were dry etched by reactive ion etching(RIE) in SF_6 plasma for silicon and CHF_3 plasma for SiO_2. The depth of the markers was measured to be over 700nm via DekTak to insure high resolution for the e-beam lithography. The UV6 resist was striped off by acetone, and then samples were further cleaned in piranha solution H_2SO_4:H_2O 2:1 for 5 minutes to remove any organic residuals. In the Piranha solution amount of sulfuric acid was higher than hydrogen peroxide to minimize oxidizing of our thin sSOI.

- Thinned HSQ:MIBK 1:1 was coated on the samples, with a two-step pre exposure bake process at 150°C and 220°C for 2 minutes each. Mesa was defined using e-beam lithography and each sample was developed for 150 seconds in MFCD-26 developer. Consequently, the samples were etched in RIE with Cl/Ar plasma to etch away the silicon between each mesa. Lastly, to suspend the nanowires, each sample was put in 1% HF solution for 5 minutes. The resulting structure is shown schematically in Figure 3.1(b). A similar process was carried out to fabricate trigate NWs using PMMA resist. However, the HF dip step was omitted to prevent underetching of the wires. Figure 3.2(a) shows a top-view SEM image of the nanowire.

- To prepare samples for deposition of the high-k/metal gate stack, they were cleaned by the full RCA process. Firstly, samples were treated in a piranha

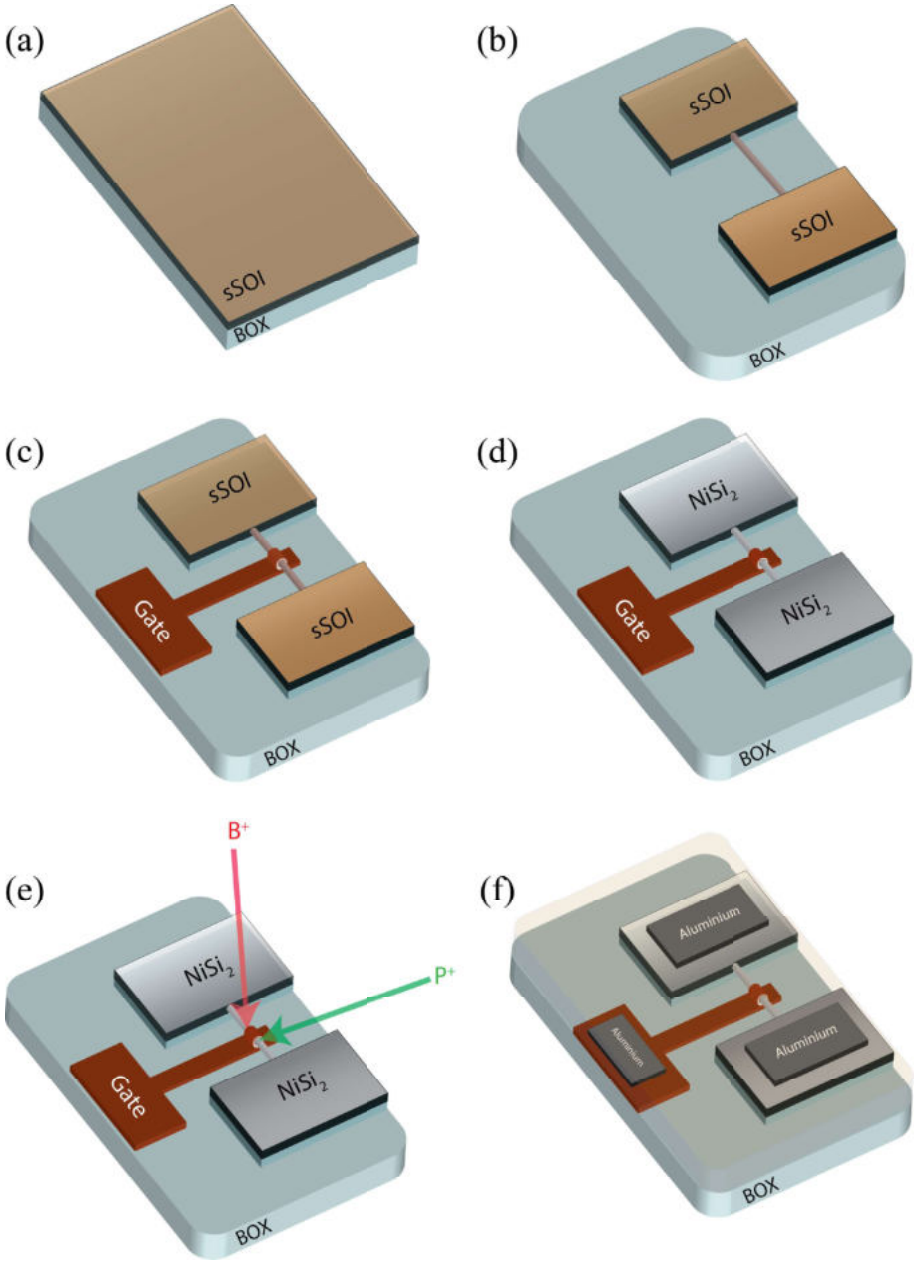


Figure 3.1: Schematics of key steps in the fabrication process.

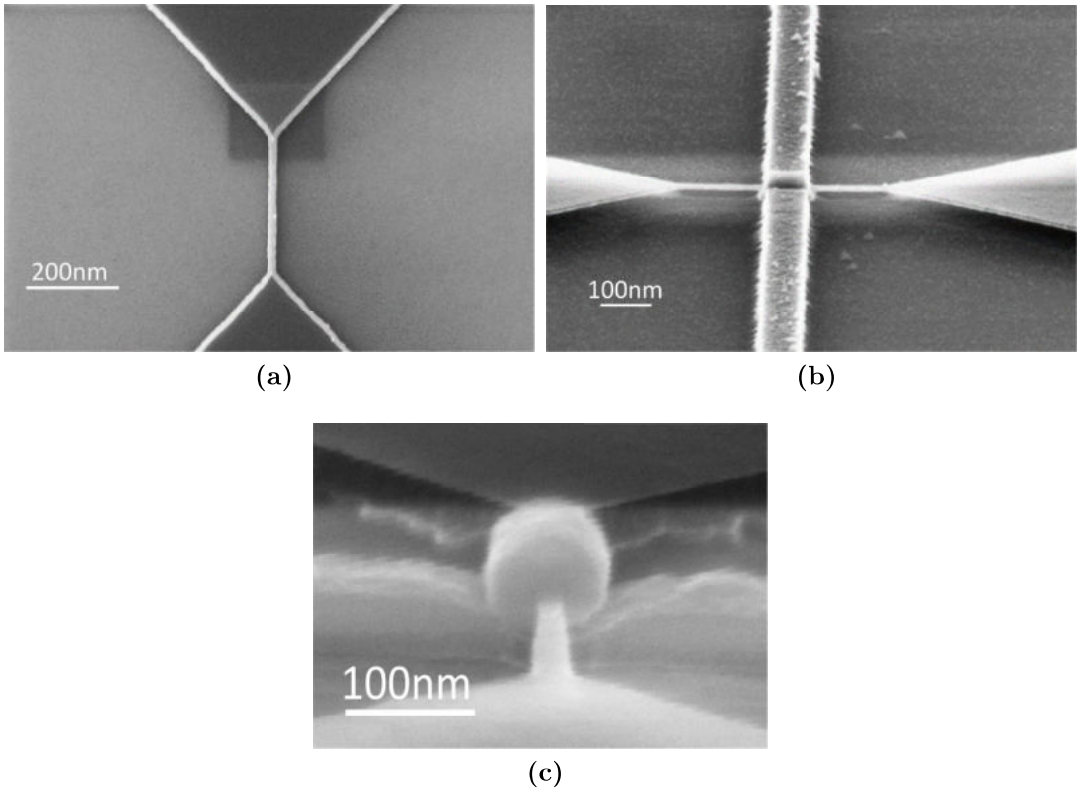


Figure 3.2: SEM images of different fabrication steps of single NW TFETs. (a) Etched and suspended single silicon nanowire on SOI substrate with dimensions of 35nm x 10nm. (b) After patterning the gate metal stack. (c) Side view of the nanowire TFET after silicidation and implantation.

solution for 10 minutes followed by a dip in 1 percent HF solution for 10 seconds to strip the oxide away. Secondly, SC1 solution with H_2O:H_2O_2:NH_4OH at 60°C was prepared and samples were cleaned in it for 10 minutes. Consequently, another HF dip for 10 seconds was carried out. Lastly, SC2 solution H_2O:H_2O_2:HCl was prepared at 60°C which samples were put in the solution for 10 minutes[51].

- Two different high-k layers of 3nm HfO_2 and 1nm Al_2O_3/2nm HfO_2 were deposited by atomic layer deposition(ALD) followed by deposition of 60nm TiN by atomic vapor deposition(AVD) or physical vapor deposition (PVD) depending on the samples. Consequently, e-beam was used to define gate area with HSQ

as mask for gate lengths of 200nm and 400nm for different transistors. The TiN layer was etched away with a combination of dry etch in RIE using SF_6/Ar gases and ICP. TiN residuals were etched away in cold SC1 solution room temperature. The resulting structure is shown in Figure 3.1(c). Figure 3.2(b) shows tilted-view SEM image of the nanowire after gate patterning.

- The next step was silicidation of nanowires to create source and drain contacts. 1.7nm Ni was deposited via PVD and subsequently annealed at 750° C to form $NiSi_2$. It is shown that this process leads to high-quality single crystalline silicide[52]. The residuals of the unreacted Ni were removed in 1:5 H_2SO_4:H_2O solution for 10 minutes(Figure 3.1(d)). The final silicide thickness can be calculated via the following formula[53]:

$$t_{\mathrm{NiSi_2}} = 3.59 \times t_{Ni} \tag{3.1}$$

  accordingly 1.7nm Ni form 6.1nm of silicide.

- Before ion implantation was carried out, the whole sample was covered with resist and implantation windows for source and drain were opened at each step. By this method, in contrast to using shadowing effect of the gate, we can avoid possible co-implantation of dopants, and allow to use different tilt angles. Furthermore,by implantation into silicide(IIS), it is possible to achieve steeper doping profiles due to dopant segregation at silicde/channel interface, as shown in [54, 55] and to decrease implantation damage to the silicon due to heavier molecules of the silicide. Boron and phosphorous ions were implanted and activated by rapid thermal annealing(RTP) at temperatures in the range of 500°C to 600°C. (Figure 3.1(e)). Figure 3.2(b) shows tilted-view SEM image of the nanowire after silicidation and ion implantation processes.

- Lastly, 100nm of PECVD SiO_2 was deposited onto the samples as passivation for metalization. Contact windows in the oxide were patterned by lithography and opened using RIE in CHF_3 plasma. The residuals of SiO_2 were etched away by HF. Samples were consequently loaded into PVD and 150nm aluminium was sputtered. Lastly, lift-off process in acetone as shown in Figure 3.1(f) was performed to form the final contacts.

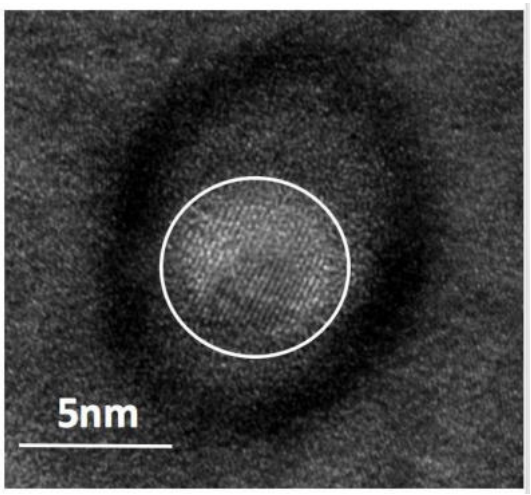


Figure 3.3: Cross-section TEM image of a NW TFET.

The transmission electron microscopy(TEM) image in Figure 3.3 shows the cross-section image of a NW TFET. It is apparent that the gate completely wraps around the highly scaled nanowire, leading to optimal electrostatic control of the channel (Chapter 2). The NW in this case is highly scaled, where the NW has diameter only of 5nm. The crystalline structure of the silicon is apparent and marked in the image.

3.3 Variability in TFETs

As devices scale down, the effect of variability on device performance becomes more and more important which needs to be studied. Among possible sources of variation geometry and dopant distribution have the highest impact on device performance. Moreover, variability considerations is an essential aspect of circuit operation by scaling devices[56, 57] which must be evaluated in detail.

Since the fabricated nanowires in this work are highly scaled, even the smallest variation in the line edge roughness(LER) can change the device characteristics[58]. As it was mentioned in chapter 2, TFET performance depends exponentially on electrostatic control which itself is dependent on geometry and gate dielectric equivalent oxide thickness. In this section, we study the effect of LER on the on-current and its relation with doping sharpness using TCAD simulations. Furthermore, we will com-

pare the simulation results with statistical data from experimental measurements.

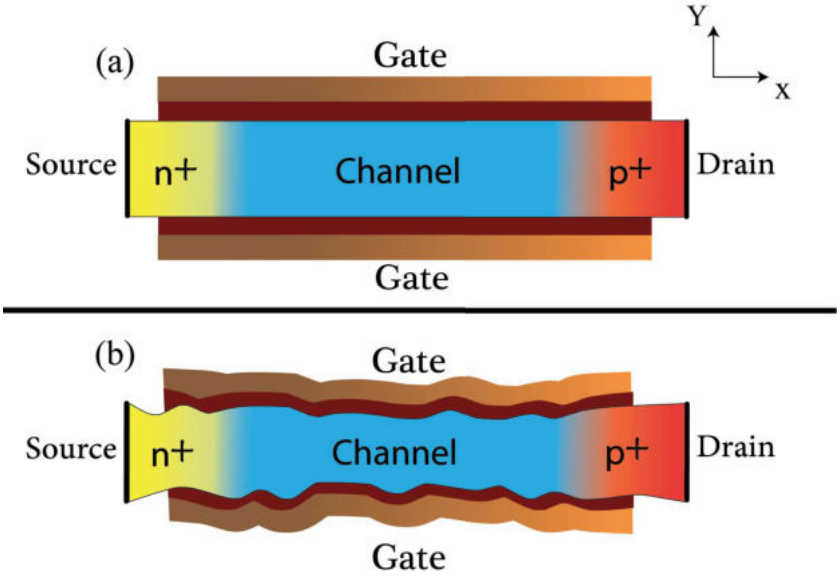
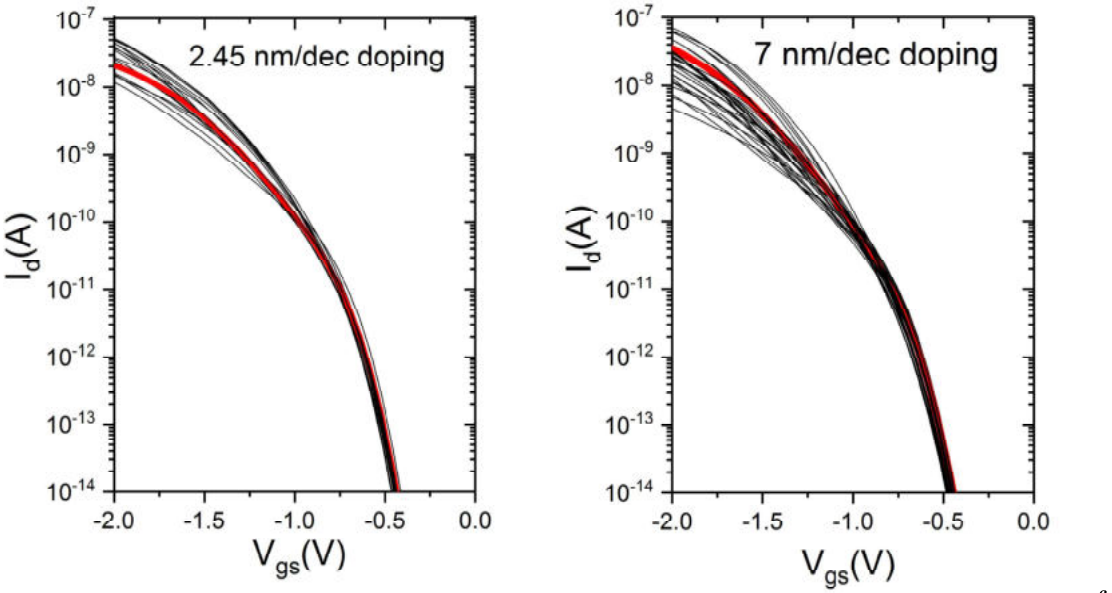


Figure 3.4: (a)Nominal structure generated by Sentaurus TCAD (b) Generated structure with random line edge roughness. In total 80 random structures were generated. Since the structure is simulated as p-TFET, n^+ is chosen as source.

3.3.1 Method of simulation

By means of TCAD device simulation, the effect of LER on transfer characteristics of TFETs was investigated. The simulation was carried out using Sentaurus technology computer aided design(TCAD). For simplicity, a 2D structure of a nanowire with two gates was considered, which is similar to a cut along the GAA nanowire TFET. As the device is biased as a p-TFET, the n^+ region is treated as source and connected to zero bias while drain and gate contacts are biased with negative values. To simulate LER, segments along the edges of nanowire were randomly moved up or down by a mean value of 2nm. The resulting structure for the nominal and LER case are shown in Figure 3.4 . The x-axis denotes direction along the nanowire, and y-axis is the nanowire thickness with dimensions of 10nmx90nm. The LER was randomized for 80 different cases and simulated for two different doping sharpness of 7nm/dec and 2.45nm/dec at the source and the drain. Models for Fermi statistics, drift-diffusion transport, doping dependent SRH generation-recombination and

non-local BTBT have been applied to self-consistently solve the Poisson equation for the structure. Parameters for the high-k dielectric and silicon were taken from the standard library of the TCAD software. It is worth noting that simulations are not meant to explicitly replicate experimental results since non-idealities as well as exact calibration of employed models have not been considered. However, it provides useful insights into device behavior.



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(a) **(b)**

Figure 3.5: Simulated transfer characteristics for devices with line edge roughness for a doping steepness of: (a) 2.45nm/dec, (b) 7nm/dec. The nominal curve is marked in red for each case.

3.3.2 Comparison of experimental and simulation results

The resulting transfer characteristics of the simulated devices for 2.45nm/dec and 7nm/dec doping profile at V_d = -0.5V are shown in Figure 3.5(a) and (b) respectively. The characteristics of the nominal case is marked by a red line in the plots. As it is evident from the figure, I_{on} current fluctuates strongly by changing LER. However, it is apparent that the variability for 2.45nm/dec case is less pronounced than for the

	mean	Standard deviation	RSD
doping profile	μI_{on}(nA)	σI_{on}(nA)	μ/σ
2.45nm/dec	90.0	48.1	1.87
7 nm/dec	14.7	14.6	1.00

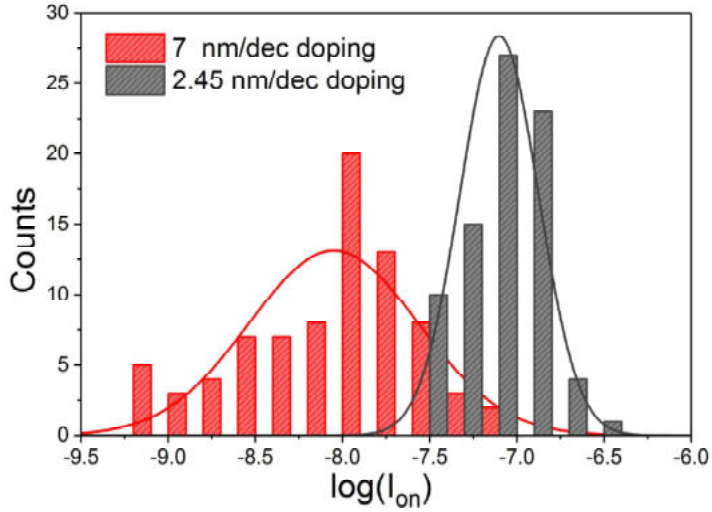


Figure 3.6: Histogram of simulated I_{on} distribution for two different doping profile. The table summarizes the normal distribution parameters mean, standard deviation and coefficient of variation.

7nm/dec case. This behavior stems from the fact that sharper doping profile limits the effect of geometric fluctuations on tunneling current to a narrower region. To quantify fluctuations, I_{on} for $V_{ds} = V_{on} = V_g - V_{off}$ = -0.5V where I_{off} = 1nA/μm was extracted and plotted in the histogram of Figure 3.6 along with a table summarizing mean, standard deviation, and relative standard deviation (RSD) for both normal distributions. For the case of 2.45 nm/dec RSD amounts to about 1.87 while for 7 nm/dec RSD is about 1.00 meaning that the distribution is worse, or in other words, broader. Moreover, the sharper doping clearly yields to higher on-currents. Obviously for the sake of circuit operation, we would like to limit the variation in a range as small as possible which requires sharp doping profiles. Theerefore, Decreasing variation as well as increasing the tunneling current can be regarded as another advantage of IIS.

In order to compare the observed trend in the simulation with experimental re-

	mean	Standard deviation	RSD
Activation temp	μI_{on}(nA)	σI_{on}(nA)	μ/σ
550°C	135.1	50.9	2.65
650°C	64.7	67.5	0.95

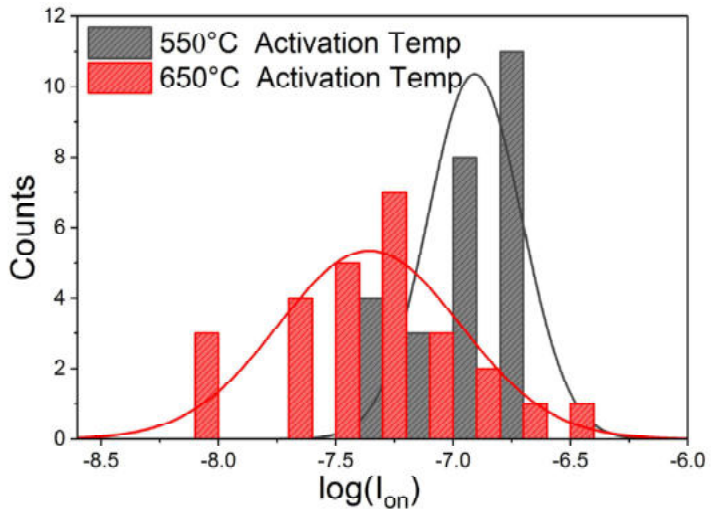


Figure 3.7: Histogram of experimental I_{on} distribution for two different activation temperatures 550°C and 650°C. The table summarizes the normal distribution parameters mean, standard deviation and coefficient of variation.

sults, single NW p-TFETs with equal fabrication condition but different activation temperature of 550° C and 650° C for 20 seconds each, were prepared and measured. For each case, I_{on} at $V_{ds} = V_{on} = V_g - V_{off}$ = -0.5V where I_{off} = 1nA/μm is extracted for 24 transistors. The resulting histogram is plotted in Figure 3.7 and a table summarizes the distribution parameters mean, standard deviation and coefficient of variation. As expected, the 550°C case forms a sharper doping profile in comparison to the 650° case. This is confirmed by the histogram and table in the figure since the p-TFET annealed at 650°C yields lower currents as well as lower RSD, meaning the distribution is broader and therefore the performance degraded. Essentially, the evidence from the experimental results confirm the simulation outcome regarding a reduction of variability in TFETs using sharper doping profile that is of utmost importance for circuit applications.

It is also worth noting that line edge roughness is not the only source of variation for real devices. Work Function Variation(WFV) is also another important factor among others which was not specifically studied. However, the experimental results in Figure 3.7 stem from cumulative effects of all variation mechanisms. In other words, the conclusion which is derived here for LER, also may apply for more general cases.

3.4 Electrical characterization of GAA Single NW Silicon TFETs

In this part, our intention is to optimize ion implantation and activation parameters for TFET characteristics. The effect of implantation dose, implantation tilt and activation temperature will be discussed. Keeping the discussion about variability in Section 3.3 in mind, in each case the best device is shown. Consequently, analogue figures of merit including transconductance g_m and output conductance g_d are extracted for the optimized device.

3.4.1 DC Characteristics

Effect of Activation

GAA single nanowire TFETs were fabricated on 15nm SOI substrate, following the process steps discussed in section 3.2. The ion implantation into silicide was carried out at 45°C tilt with phosphorous ions to a dose of 5×10^{15}cm^{-2} and at 3keV energy along boron ions at a dose of 5×10^{14}cm^{-2} with 1.5keV energy. The reason for using lower dose of boron is to suppress the ambipolar branch in the p-TFET owing to a higher Schottky barrier for electrons at the $NiSi_2$ silicide[59]. To avoid intermixing of dopants, for each step of the implantation a window using PMMA resist and e-beam lithography was opened. To activate the dopants, rapid thermal annealing was used at 550°C and 650°C for duration of 20 seconds on different samples. These devices are referred to as Set1.

The resulting transfer characteristics $I_d - V_{gs}$ of the fabricated TFETs are shown in Figure 3.8(a), biased in p-TFET mode. The transistor with lower activation temperature shows higher on-current of 8.54μA/μm with respect to 3.94μA/μm for devices with higher activation temperature. This is due to extended diffusion of dopant, in

this case phosphorous, diffuse further at higher temperature resulting in a broader doping profile. In other words, higher temperature anneal creates longer tunneling distances (higher λdop) from source to channel, decreasing tunneling probability T(x) according to the WKB approximation(Chapter 2). Also Figure 3.8(b) shows a SS vs I_d plot for the discussed cases at $V_d = -0.1V$ with considerable improvement in minimum and average SS for the case with lower activation temperature. It is worth noting that SS was extracted for higher I_d currents than the gate leakage current and at $V_d = -0.1V$ since higher V_d deteriorates SS due to a tunneling contribution from drain. To gain more insight, output characteristics $I_d - V_{ds}$ of Set1 of devices are shown in Figure 3.9 for both cases at $V_{ov} = V_{gs} - 0.5V$. The output characteristics show good saturation but it also displays a super-linear onset for low V_d. Presumably the super-linear onset of the TFET output curve is caused by drain induced barrier thinning[27] or by a deviation of occupancy function at the starting point and the edge of the tunneling probability energy window as discussed in [47]. In any case, it is demonstrated that the disparity of current by changing V_{ds} decreases remarkably due to a higher doping concentration. Based on this concept, for Set1 devices at both cases, a deficit of active dopant concentration at source is apparent although the source was implanted with high dose of 5×10^{15} p^+ cm^{-2}. This could be caused either by high activation temperature or activation time being too long or a combination of these reasons.

To scrutinize our assumption, a different set of devices with $1 \times 10^{15} cm^{-2}$ for phosphorous and boron implantations at energies of 3keV and 1.5keV respectively were fabricated. Based on the results inferred from Set1, these devices were activated at 550°C for 10 seconds, half of the activation time used for Set1. The nanowire dimensions are equal to the previous case. These devices are referred to as Set2. The transfer characteristics for n-TFET and p-TFET for $|V_d| = |0.3V|, |0.5V|$ show that due to higher boron implantation dose with respect to Set 1 the ambipolar branch is much stronger(Figure 3.10(a,b)). p-TFET shows an I_{on} of $2.41 \mu A/\mu m$ and n-TFET an I_{on} of $0.78 \mu A/\mu m$ for $V_{ds} = V_{on} = V_g - V_{off}$ = -0.5V where I_{off} = 1nA/μm leading to an I_{on}/I_{off} ratio of 2.41x10^3 and 0.78x10^3, respectively. Furthermore, in case of the p-TFET, the minimum SS has also improved from 68mV/dec to 63mV/dec with respect to Set1. However, the n-TFET shows worse SS than the p-TFET. This is caused by a broader tunneling junction due to higher boron diffusion at source of the n-TFET.

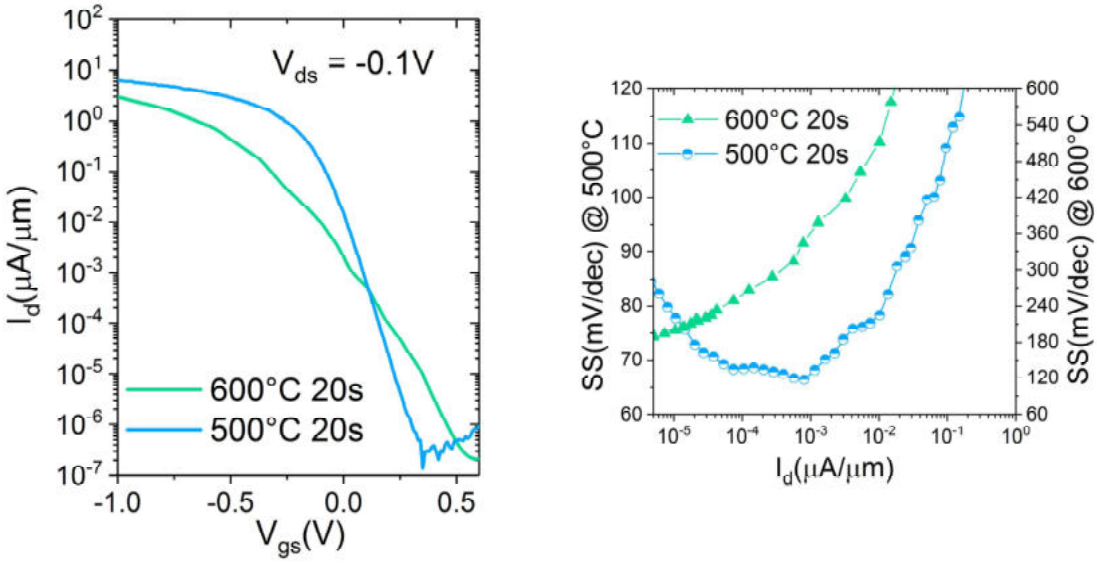


Figure 3.8: (a) Measured transfer characteristics $I_d - V_{gs}$ and (b) SS versus I_d plots for Set1.

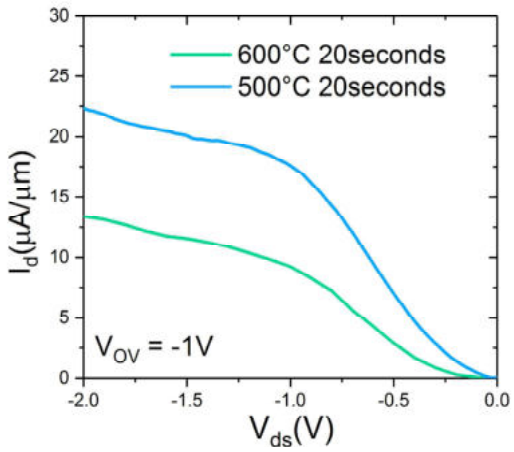
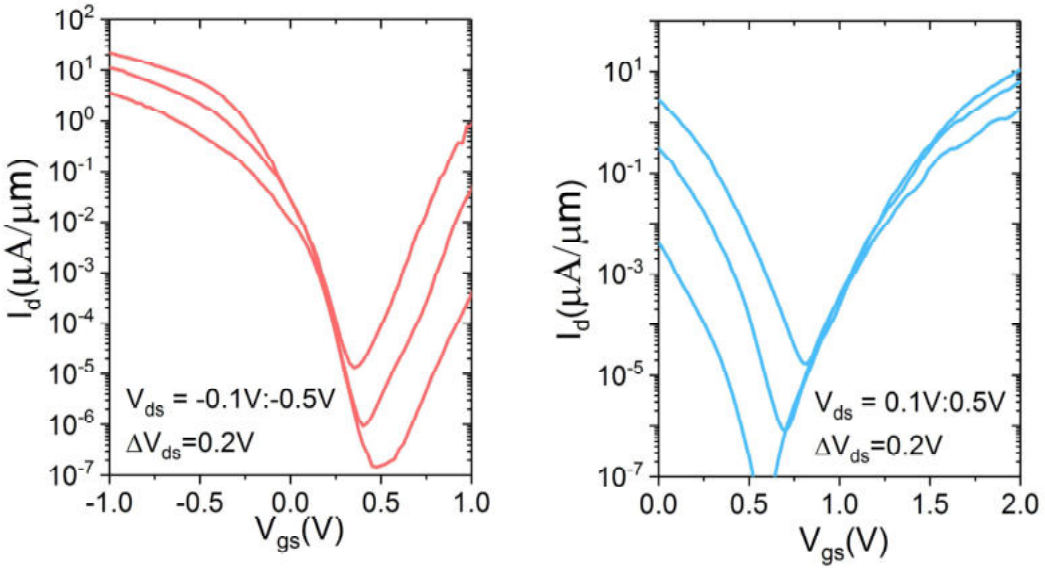


Figure 3.9: Measured output characteristics of Set1 transistors for two different activation temperature at 500°C (blue) and 600°C (green).

The output characteristics of Set2 p-TFET and n-TFET are shown in Figure 3.11(a) and (b), respectively. In case of p-TFET, the characteristics do not show super-linear onset at low V_d anymore. This indicates that the activation temperature and du-

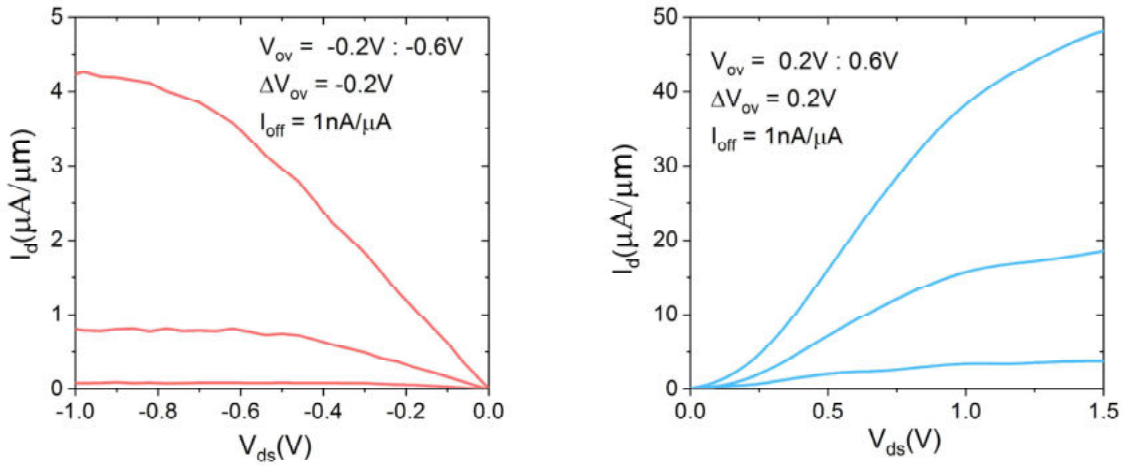


(a) **(b)**

Figure 3.10: Measured transfer characteristics I_d-V_{gs} of Set2 devices for (a) p-TFET and (b) n-TFET.

ration have lead to higher dopant concentration at the source. However, in case of the n-TFET, it still exhibits the super linear onset. This is due to higher diffusion coefficient of boron in silicon with respect to phosphorous which has lead to lower dopant concentration and subsequently higher variation of current by changing V_{ds}. This finding is also aligned with inferior SS of the transfer characteristics of Set2 n-TFET in Figure 3.10(b). Furthermore, both devices show good current saturation, especially the p-TFET due to its superior doping profile at the source.

Based on the results from Set1 and Set2, it is apparent that for n-TFETs the boron doped junction should be optimized. In order to achieve this goal a set of devices with different doping processes were fabricated. The ion implantations were carried out at an angle of 0° as opposed to the former 45° tilt, to make a larger gap between the ions and the channel/silicide interface. In this way, the dopants will diffuse less into the channel due to the larger distance to the interface. The single NW n-TFET has a dimension of $30nm \times 10nm$ with 3nm ALD HfO_2 and 60nm AVD TiN. The boron and phosphorous implantations were carried out with a dose of 1×10^{15}cm^{-2}



(a) (b)

Figure 3.11: Measured output characteristics I_d-V_{ds} of Set2 devices for (a) p-TFET and (b) n-TFET.

with zero tilt. The activation based on the results from Set2 was done at 500°C for 10 seconds. Hereafter, these devices are called Set3.

The DC Transfer characteristics I_d-V_{gs} of Set3 n-TFET are plotted in Figure 3.12 for three different V_d values. The device shows great improvements in the n-branch and the ambipolar behavior is weaker in comparison. This can be attributed to lower activation temperature and zero implantation tilt, considering that phosphorous diffuses less than boron in silicon. The device exhibits very good subthreshold behavior with average SS of 76mV/dec over four orders of I_d. Moreover, the I_{on} current has greatly improved. I_{on} current of 15 μA/μm and 10.7 μA/μm are achieved for $V_{dd} = V_{ds} = V_{on} = V_g - V_{off} = 0.5$V at $I_{off} = 1$nA/μm and $I_{off} = 100$pA/μm, resulting in an I_{on}/I_{off} ratio of 1.5e4 and 1.07e5, respectively.

The corresponding output characteristics of Set3 n-TFET is shown in Figure 3.13.There is no super-linear onset meaning the source junction concentration is in the optimum range to avoid this negative behavior. Furthermore, the device displays very good current saturation.Table 3.1 summarizes the fabrication parameters and the device performance numbers.

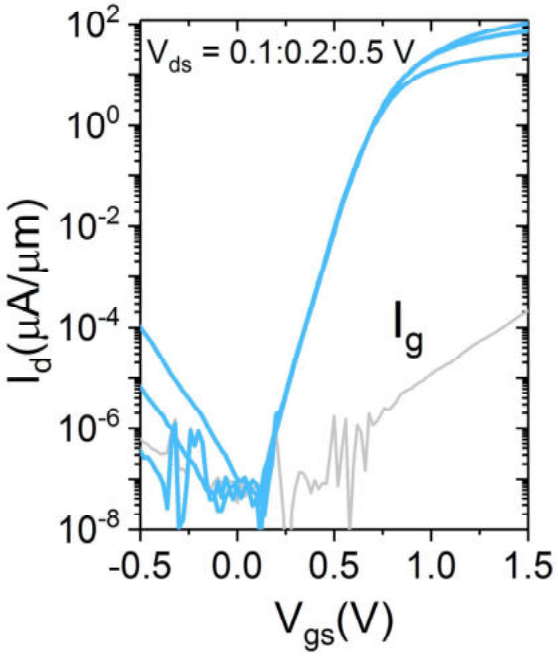


Figure 3.12: Measured transfer characteristics I_d-V_{gs} of Set3 n-TFET. The gate leakage I_g is shown in gray color.

Set	Implantation	Activation	I_{on} μA/μm	SS_{avg} mV/dec	Linear onset
pTFET (Set1)	P $1x10^{15}cm^{-2}$ 45° B $5x10^{14}cm^{-2}$ 45°	500°C 20s	8.52	84	No
pTFET (Set1)	P $1x10^{15}cm^{-2}$ 45° B $5x10^{14}cm^{-2}$ 45°	600°C 20s	3.94	126	No
pTFET (Set2)	P $5x10^{15}cm^{-2}$ 45° B $1x10^{15}cm^{-2}$ 45°	550°C 10s	2.41	102	Yes
nTFET (Set2)	P $5x10^{15}cm^{-2}$ 45° B $1x10^{15}cm^{-2}$ 45°	550°C 10s	0.78	153	No
nTFET (Set3)	P $1x10^{15}cm^{-2}$ 0° B $1x10^{15}cm^{-2}$ 0°	500°C 10s	15	76	Yes

Table 3.1: A summary of different implantation and activation parameters and the corresponding device results.

Analogue characteristics

TFETs have advantages for certain analog applications compared to MOSFETs for low power circuit design. In this regard, an important parameter is g_m/I_d ratio or

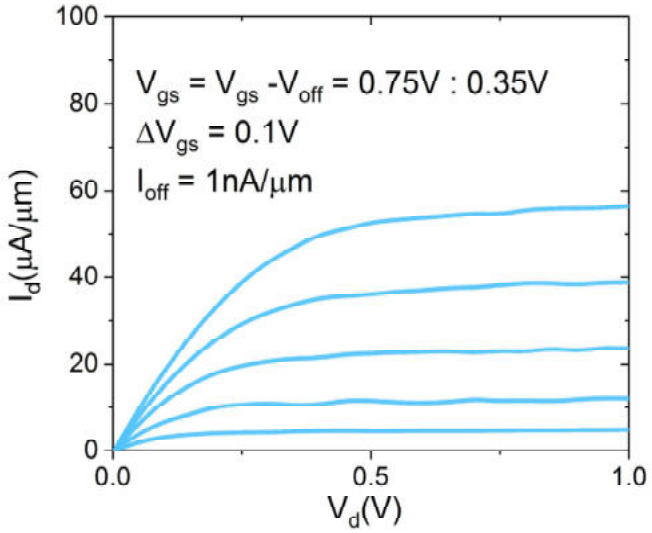


Figure 3.13: Measured output characteristics of transistor Set3 n-TFET for different values of V_{ov}. The device shows very go od I_{on} of 15μA/μm at $V_{dd} = 0.5V$ and very good saturation.

transconductance efficiency[60], in which $g_m = \frac{\partial I_d}{\partial V_{gs}}$ is called transconductance, a parameter showing how much control V_{gs} over I_d has. The transconductance efficiency is equal to ln(10)/SS [61]. This basically means that the transconducance efficiency of TFETs can be superior to that of MOSFETs at certain currents due to the ability of TFET at achieving SS smaller than 60mV/dec at room temperature. However, this usually happens at low currents. Therefore, low frequency analogue applications are the most suitable to take advantage of this phenomenon.Another important analogue parameter is the output resistance of TFETs calculated as $r_o = 1/\ g_d = [\ I_d/\ V_d]^{-1}$ where g_d is the output conductance. The g_d of a TFET in saturation region is determined mostly by BTBT at the source with small impact from drain voltage[62]. Consequently, the output resistance of TFETs is high leading to large intrinsic voltage gain($A_V = g_m/\ g_d$). In this section, we will calculate analogue figure of merits for transistor T3 shown in Figure 3.12 as our optimized n-TFET in order to directly compare it to the previously optimized NW array n-TFET supplied by Luong et al in [63], which has been fabricated with the same technology.

Figure 3.14 demonstrates the calculated g_m versus V_{ov} for different V_{ds}, where $V_{ov} = V_g - V_{off} = 0.5$V, for an I_{off} of 1nA/μm. As g_m basically shows the gate control,

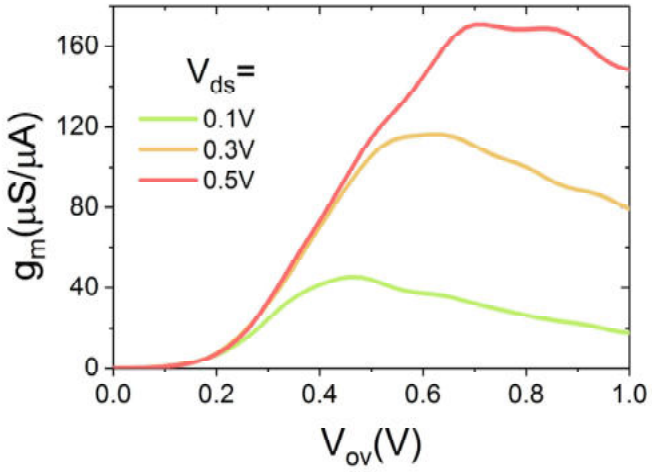


Figure 3.14: Extracted transconductance g_m for the sSi single NW GAA n-TFET shown in Figure 3.12 different V_{ds} values.

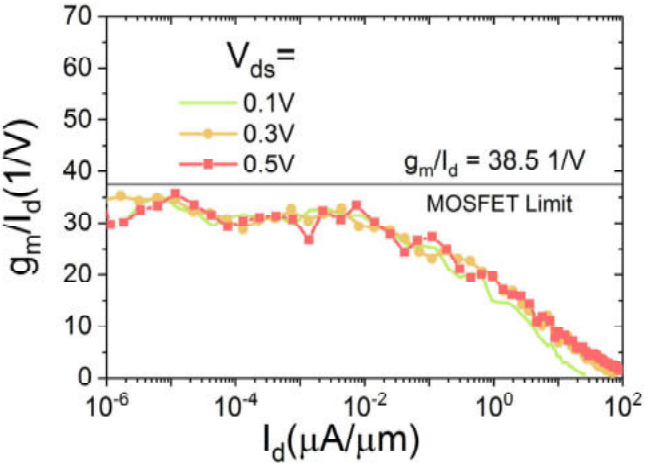


Figure 3.15: Extracted transconductance efficiency g_m/I_d for sSi single NW GAA n-TFET shown in Figure 3.12 as a function of drain current I_d for different V_{ds} values.

electrostatics and geometry of the device play an important role in determining its value. Accordingly, one would expect that a NW TFET to show higher g_m than a planar TFET. As shown in the figure, the calculated transconductance has a value of $g_m = 44\ \mu\text{S}/\mu\text{m}$ at $V_{ds} = 0.1\text{V}$ where for the nTFET device in [63], g_m has a maximum value of $18\mu\text{S}/\mu\text{m}$ at the same V_{ds} level. Therefore, Set3 shows more than

twice improvement. The transconductance reaches a maximum value of 170μS/μm for $V_{ds} = 0.5$V.

The transconductance efficiency g_m/I_d is shown in Figure 3.15 plotted versus I_d for different V_{ds}. It shows constant value of around 30V^{-1} over a wide range of current as opposed to 23V^{-1} for n-device in [63]. Since this particular device does not show SS lower than 60mV/dec it is worth mentioning that the transconductance efficiency is limited to the MOSFET range.

Derivatives of g_m can be used to assess nonlinearity of the drain current in analog circuits. It is shown that a Taylor expansion of I_d around V_{gs} yields [64, 65]:

$$I_d(V_{gs}) = g_m V_{gs} + \frac{1}{2} a_{2_{gm}} V^2{}_{gs} + \frac{1}{6} a_{3_{gm}} V^3{}_{gs} + ... \tag{3.2}$$

where the coefficients are partial derivatives of g_m as:

$$a_{2_{gm}} = \frac{\partial^2 I_d}{\partial V_{gs}^2} = \frac{\partial g_m}{\partial V_{gs}} \tag{3.3}$$

$$a_{3_{gm}} = \frac{\partial^3 I_d}{\partial V_{gs}^3} = \frac{\partial^2 g_m}{\partial V_{gs}^2} \tag{3.4}$$

Figure 3.16 shows the calculated $\frac{\partial g_m}{\partial V_{gs}}$ versus V_{ov1} and $\frac{\partial^2 g_m}{\partial V_{gs}^2}$ versus V_{ov2} for the n-TFET from set3 at $V_d = 0.3V$. As it is apparent both terms decrease rapidly to small values where by $V_{ov} = 0.3V$, very good higher order linear behavior for I_d is observed.

The output conductance g_d of the n-TFET is plotted in Figure 3.17, which reflects the excellent current saturates by increasing V_d. As shown g_d increases to a value of 110μS/μm for $V_{ov} = 0.55$V then drops to very small values indicating very good current saturation. Moreover, intrinsic voltage gain $A_V = 175$ at about $V_{ov} = 0.35$V is obtained which is considerably higher than state of the art NW array n-TFET in [63] achieving $A_V = 20$ at $V_{ov} = 0.3$V due to the process optimization.

3.5 Effect of trap assisted tunneling

Several different TFET designs employing various material from group IV and group III-V have been proposed and fabricated. However, only a small number of them have achieved sub-60 mV/dec subthreshold slope SS at room temperature and only

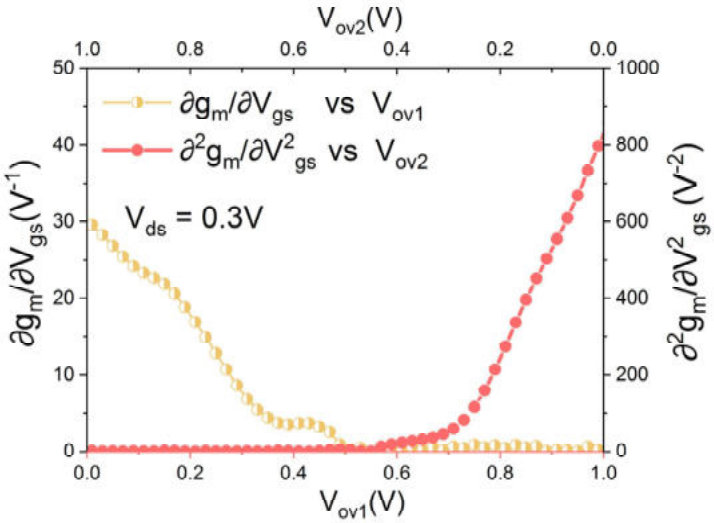


Figure 3.16: Calculated $\frac{\partial g_m}{\partial V_{gs}}$ and $\frac{\partial^2 g_m}{\partial V_{gs}^2}$ terms for the sSi single NW GAA n-TFET shown in Figure 3.12. Both terms drop to small values indicating good higher order linearity of I_d, particularly important for analog circuit design.

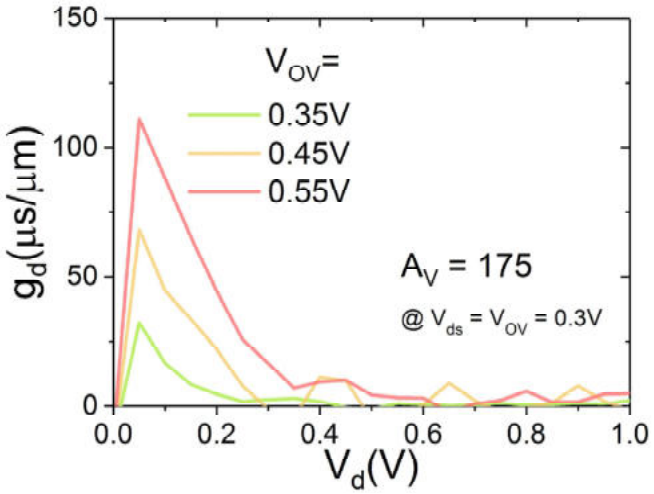


Figure 3.17: Calculated output conductance g_d for the sSi single NW GAA n-TFET shown in Figure 3.12 dropping to small values revealing good current saturation. A high voltage gain, $A_V = 175$ at about $V_{ov} = 0.3$V is obtained

at small current values [66, 67, 68, 69, 70]. According to the theoretical TFET operation, current starts to flow only when there is an overlap between valence band of the source and conduction band of the channel, that is achieved by a specific voltage depending on physical conditions. This certain voltage is called BTBT threshold voltage. However, in reality there are some non-ideal effects that cause current flow before this overlap is achieved, for example gate leakage, trap assisted tunneling [71, 72], or band-tails in the density of states that decay exponentially into the bandgap [73, 74]. According to the WKB approximation, the steepest current change due to BTBT occurs at the beginning of the overlap, or hence at low currents. Therefore, non-ideal currents mask the steepest part of the subthreshold slope SS and practically degrade TFET characteristics. It has already been shown that subthreshold switching of fabricated TFETs has remarkable temperature dependence while ideal TFET does not show subthreshold temperature dependence, as shown in Chapter 2. This points out to evident thermionic parasitic processes. Moreover, it has already been demonstarted that among possible effects TAT is a major thermionic component of subthreshold switching of TFET current [44]. Trap assisted tunneling could stem from oxide-channel interface traps or from traps in the semiconductor itself. In this section, we experimentally determine the interface trap density of states and evaluate effects of the fabrication process on it. Furthermore, we will measure high and low temperature transfer characteristics of GAA single NW TFET in order to investigate temperature dependent processes. Lastly, the energy level of traps in the bandgap are estimated from the measurements.

3.5.1 Density of interface traps

A straight forward yet precise approach to measure density of interface traps is to use the charge pumping method that was first exhibited by Brugler et al in 1969 [75]. However, it was not until 1984 that Groeseneken et al[76] supplied thorough explanation of its working principle, turning it into a reliable measurement tool. From this measurement, crucial data about quality of oxide interface by measuring interface traps density D_{it} can be inferred. The charge pumping method was originally used on bulk FET devices, where source and drain were reversed biased and pulse current between gate and body contact was measured. However, the original method due to absence of bulk contact on SOI NW devices is not directly applicable. It was shown by Elewa et al[77] that gated p-i-n diodes can be measured using the charge pumping

method, making the approach relevant to NW TFETs.

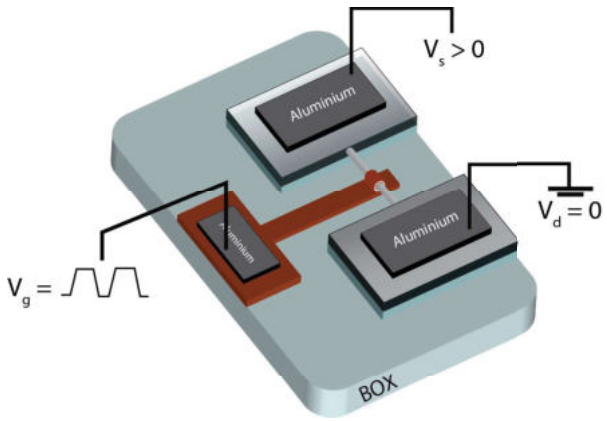


Figure 3.18: Schematics of charge pumping measurement setup for a NW TFET. The source contact is reverse biased while keeping the drain at zero volt. Trapezoidal voltage pulse is applied to the gate, by varying V_{base} changing the device condition between accumulation and inversion.

In order to measure I_{cp} current, as shown in Figure 3.18, the nanowire TFET source was connected to a small reverse voltage while the drain contact was kept at zero volt. Thereupon, a trapezoidal voltage pulse is applied to the gate, by varying V_{base} changing the device condition between accumulation and inversion.

Five different zones can be spotted in I_{cp} current. Figure 3.19(a) marks each zone along the relevant bias zones in Figure 3.19(b). As shown, V_{base} is swept to steer the device from accumulation condition to inversion. First, if the whole pulse is under the V_{fb} voltage, no recombination I_{cp} current is measured since the traps are lastingly filled. Second, top of the pulse reaches between V_{th} and V_{fb} driving the device into depletion to maximum weak inversion causing the I_{cp} to increase. Meanwhile, the V_{base} is around V_{th} - t_{base}. Third, top of the pulse is above V_{th} and bottom above V_{fb}. In this zone, the pulse changes condition from accumulation to deep inversion and back. This causes the negative and positive carriers to fill in traps and consequently recombined giving rise to a specific maximum I_{cp}. Fourth, the V_{base} is higher than V_{fb} and lower than V_{th}. In this zone, the transistor does not reach strong accumulation and interface traps are chiefly negatively filled leading to reduced recombination and lower I_{cp} current. Lastly, V_{fb} is larger than V_{th}, keeping the device in strong inversion. It means the traps are lastingly filled and no recombination happens and I_{cp} is nearly zero, except for parasitic leakage currents. It is shown that by measuring current at

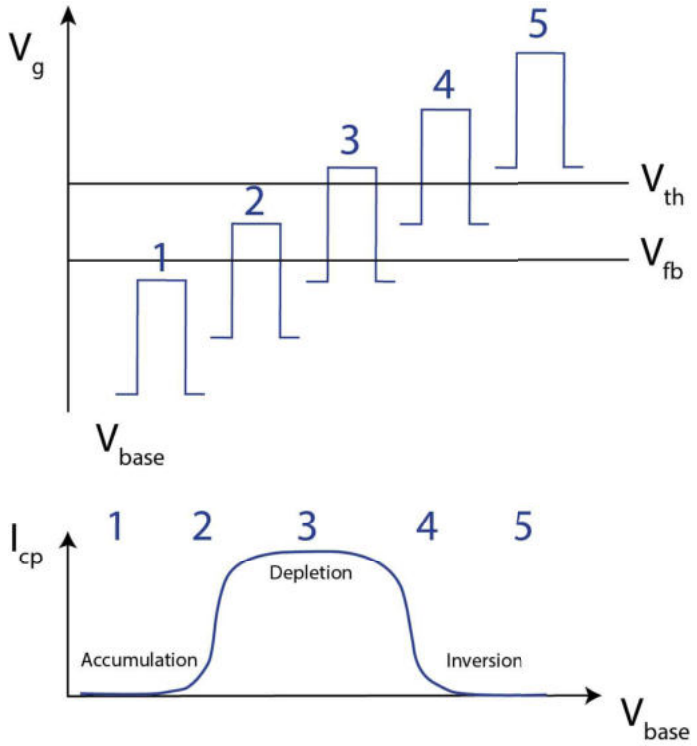


Figure 3.19: Various zones when sweeping V_{base} in charge pumping measurement. As the base crosses V_{fb} and V_{th}, it gives rise to 5 different operation zones marked by numbers 1-5 in the plot.

low frequency, it is possible to subtract the parasitic contribution from the I_{cp} current measured at high frequency[78]. By taking the maximum of I_{cp} current, the following relation holds:

$$I_{cp} = qfWL_gN_{it} \tag{3.5}$$

where N_{it} is the number of oxide and interface traps per area, W the width, L the length of the gate, q the electron charge and f pulse frequency. Moreover, from N_{it} the interface trap density D_{it} can be calculated as:

$$D_{it} = N_{it}/\Delta E \tag{3.6}$$

where ΔE is the difference between the accumulation and inversion levels.

For these measurement TFETs with an array of 20 nanowires were fabricated. TFETs employ 3nm HfO_2 as dielectric and 70nm PVD TiN as gate metal. However,

is has already been shown than PVD TiN could exert significant oxide damage[79]. However, R. Choi et al[80] have shown that forming gas(FG)(N_2 + H_2) annealing can amend these damages. In this part, we seek to measure N_{it} for before and after FG annealing and compare the results with each other. For this purpose, the device was treated at 400°C for 10 minutes in FG in an RTP chamber.

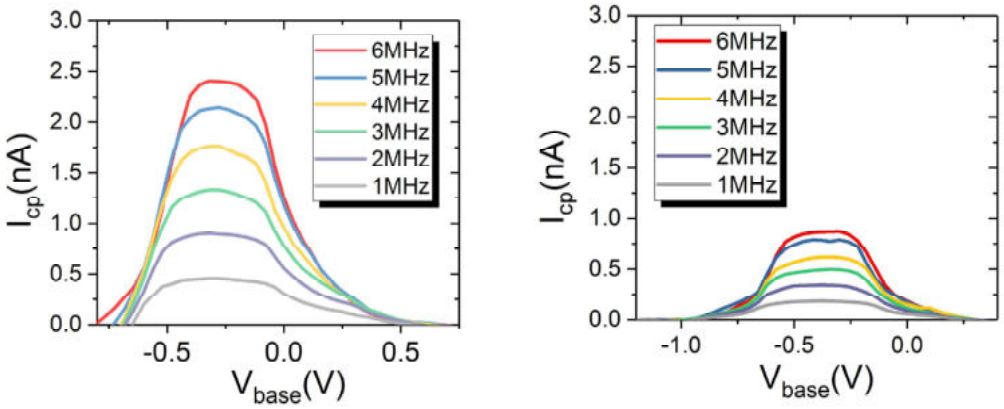


Figure 3.20: I_{cp} current versus V_{base} for (a) before FG annealing (b) after FG annealing.

I_{cp} was measured at frequencies from 1MHz to 6MHz for devices without and with FG anneal as shown in Figure 3.20(a) and (b), respectively. As the frequency increases, the fast charging traps recombine more frequently causing higher I_{cp} current. The N_{it} calculation is normalized to the measurement frequency. It is evident from the figure, that FG anneal has greatly reduced the I_{cp} current, corresponding to N_{it} = 2.83x10^{12}cm^{-2} before FG and N_{it} = 7.41x10^{11}cm^{-2} after FG (D_{it} = 2.32x10^{12}cm^{-2}//eV and D_{it} = 6.61x10^{11}cm^{-2}//eV, respectively). Clearly the high-k - Si interface is greatly improved. S.Richter[81] showed that by using AVD TiN a better D_{it} value(close to the measured value here) is achievable even without FG anneal. Decreasing D_{it} is imperative to achieve lower I_{off}, better I_{on}/ I_{off} ratio, lower V_{th} voltage and better SS value[82].

3.5.2 Low Temperature I-V characteristics

In the direction of drawing deeper insights into temperature dependent processes, single NW silicon GAA TFETs were fabricated, and cooled down to 100K in a custom setup using liquid nitrogen. In order to achieve low D_{it} values, as discussion in the previous section, 60nm AVD TiN deposited as metal gate. Moreover, to minimize traps caused by implantation, dopant activation was carried out at high temperature 700°C for 10 seconds. The resulting measurement is shown in Figure 3.21(a) for temperatures ranging from 400K to 100K. In the subthreshold region, TFET shows strong temperature dependency in a way that by decreasing temperature, SS greatly improves and onset voltage also increases. This is due to freeze out of thermionic TAT process which mask the tunneling contribution at small currents. Figure 3.21(b) shows the minimum SS vs T plot for further comparison along the theoretical MOSFET line. As opposed to the MOSFET limit, SS of TFET does not decrease linearly, indicating rapid reduction in contribution of TAT until 200K. A freeze out of traps happens at around 140°K as SS value tends to become constant. Other processes like temperature dependence of phonon assisted tunneling of BTBT in indirect semiconductors also could affect the characteristics, however, at small currents, TAT is the dominant effect. In the on region of the transfer curve, I_{on} current increases by increasing temperature. As in this region, BTBT mechanism is dominant, and according to WKB approximation it exponentially depends on the bandgap E_g , the increase of the I_d-current can be explained by the following term which explains bandgap as a function of T[83]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{3.7}$$

α and β are material specific constants. According to the formula, as temperature increases, E_g decreases which results in exponential increase of I_{on} current. However, it should be noted this behavior continues up to a point where voltage drop over channel resistant R_{resist} due to I_{on} is negligible, otherwise, a reduction with temperature would be measured[84]. This is especially true for higher V_{ds} voltages since they result in higher initial I_{on}. In order to further investigate the effect of traps activation energy E_a has been derived from temperature dependent I-V measurements. Activation energy basically describes how much sensitivity to temperature does current have at a specific V_{gs}. Generally, as rule of thumb values below $E_a < 0.1eV$ are considered to

be dominated by BTBT. For E_a values around half-bandgap dominant mechanism is considered to be Shockley-Read-Hall recombination. E_a is calculated from Arrhenius plot through the following relation:

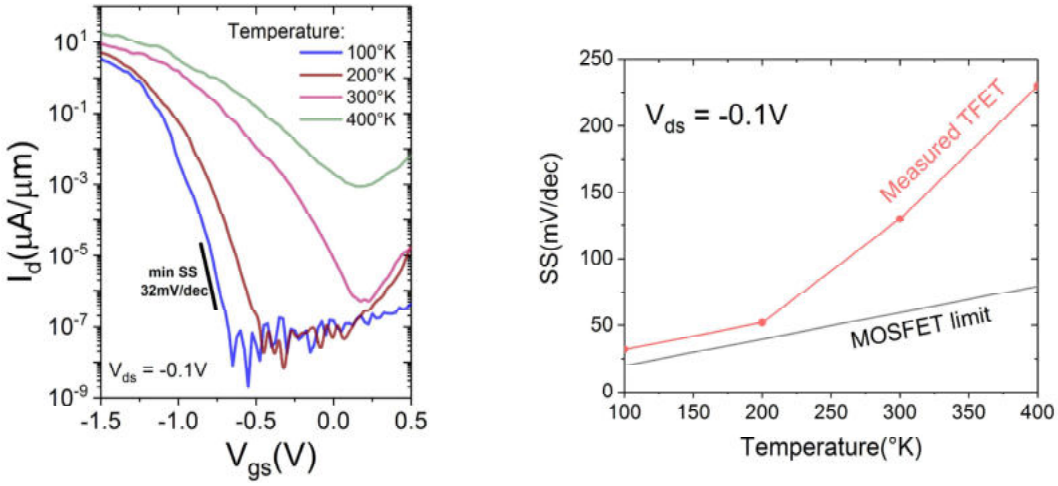


Figure 3.21: Transfer characteristics of silicon GAA single NW p-TFET with NW dimension of 35nmx10nm and gate length of 350nm measured for temperatures ranging from 400°K to 100°K)(b) Measured minimum SS of the p-TFET as a function of T temperature. The theoretical limit of SS for MOSFETs is also shown for comparison.

$$I_d \propto exp(\frac{E_a}{k_B T}) \tag{3.8}$$

where the plot is obtained by taking the natural algorithm of the relation and drawing $\ln(I_d)$ versus $1/k_bT$ for each specific V_{gs} at a specific V_{ds} = -0.1V. The slope of the resulting lines is the activation energy Ea. By plotting it against its respective V_{gs} the Figure 3.22 is obtained where different conduction mechanisms are marked in the plot, where BTBT is the dominant mechanism for voltages greater than |0.57|. Transition from TAT to BTBT occurs in a gate voltage window δV_{gs} of 0.61V, indicating non-negligible TAT contribution. This value is still smaller than TFETs with SiGe or Ge source material, due to larger and indirect bandgap of silicon.

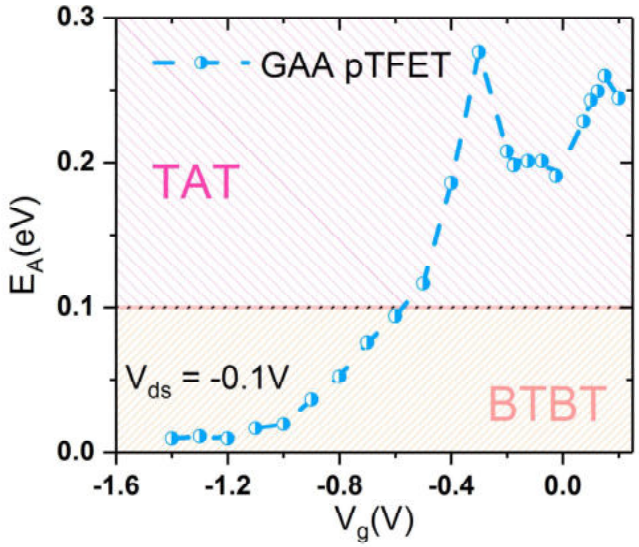


Figure 3.22: Activation energy plot

3.5.3 Energy level of traps

As discussed in the previous section, thermal excitation of charge carriers occurs from the trap states into the conduction band [85]. There is consensus that trap assisted tunneling can be modeled as Pool-Frenkel emission given by [86, 85]:

$$I_d/V_{gs} \propto exp(\frac{q}{k_B T}(2a\sqrt{V_g s} - \phi_B)) \tag{3.9}$$

where $a = \sqrt{\frac{q}{4\pi\epsilon_o x d}}$ and ϕ_B is the barrier height. By taking the natural logarithm of the equation and plotting $ln(I_d/V_{gs})$ versus $\frac{1}{k_B T}$, the slope of the resulting line C is equal to:

$$C = -\phi_B + 2a\sqrt{V_{gs}} \tag{3.10}$$

To carry out the calculations, $V_{gs} = -0.4$ was chosen according to Figure 3.22 to make sure TAT is the dominant mechanism. Figure 3.23 shows the plot for extraction of the barrier height. Our dielectric comprises of 1nm interfacial SiO_2 and about 3nm HfO_2 corresponding to the equivalent oxide thickness d = 1.54nm. From the data $-\phi_B = 0.53eV$ is derived which basically is the energy difference of traps with respect

to channel valence band, as it is modeled with a potential well.

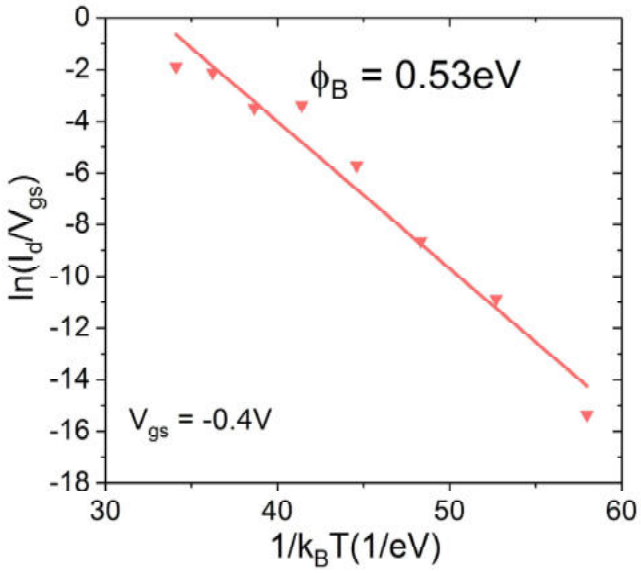
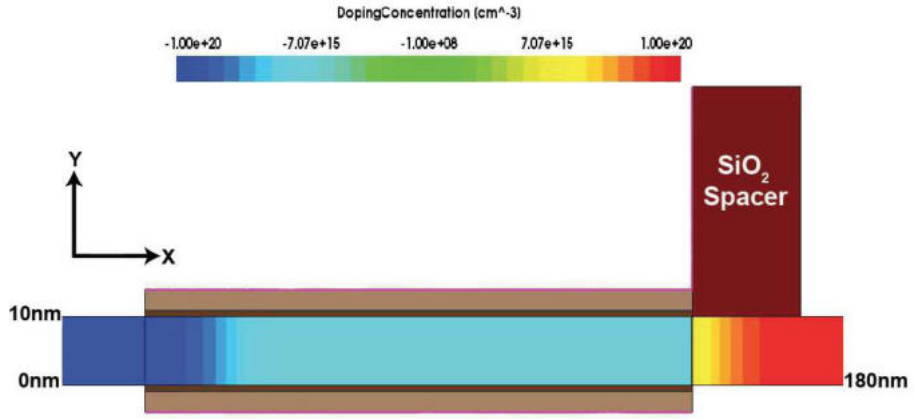


Figure 3.23: Extracted barrier height ϕ_B for thermal excitations from trap states.

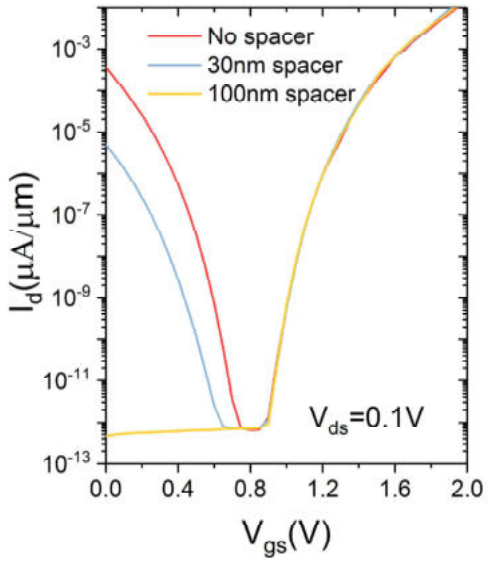
3.6 Suppression of the ambipolar behavior

As already shown, it is possible to suppress the ambipolar behavior by asymmetric doping of pTFETs. However, since this method is not applicable for suppression of nTFET ambipolarity, it is not a suitable design for complementary digital circuits where both n- and p-TFETs are needed for energy efficient operation. Therefore, in order to systematically suppress the ambipolar behavior, we will leave an intrinsic region between drain and channel, called drain-channel underlap. This method effectively worsens the drain junction which leads to suppression of the ambipolar behavior. This concept has been shown by simulation in Figure 3.24(a) where a certain gap between drain and channel is created by deposition of SiO_2. In the simulation, this gap was varied in length in order to evaluate its effect more closely. Figure 3.24(b) depicts the DC transfer characteristics I_d-V_{gs} of the simulated nTFET with different gate-drain underlap lengths. By increasing the underlap length, the ambipolar be-

havior also decreases by an underlap of 100nm only the gate leakage current remains, with no ambipolar conduction, even at highly negative V_{gs} voltages.



(a)



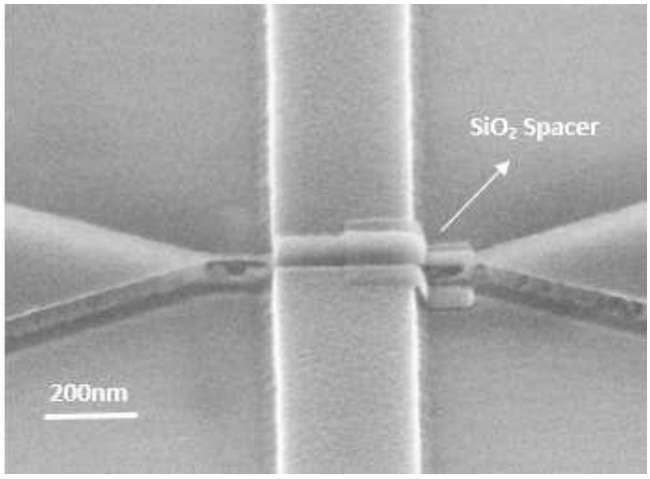
(b)

Figure 3.24: (a) 2D simulation structure of nTFET with drain-gate underlap created via SiO_2 deposition on the drain side. (b) Effect of drain-gate underlap length on the ambipolar branch of the simulated nTFET.

In order to transfer this concept into our design, we have added some additional

process steps between (c) and (d) in Figure 3.1. Firstly, 50nm PECVD SiO_2 was deposited on the samples. In order to protect the oxide on the drain side from being etched away, we also deposited 5nm TiN, by AVD for maximum conformity, as a hard mask. Then TiN was patterned on the drain side using HfO_2 and the rest was etched off chemically in SC1 solution. Consequently, 1% HF dip for a minute removed all the SiO_2, except those on the drain side protected with the TiN. The process steps are shown in the Figure 3.25(a) and the final structure SEM in Figure 3.25(b). After the gate-drain underlap is formed, the rest of the fabrication process is the same as described in Section 3.2.

(a)



(b)

Figure 3.25: (a) Fabrication steps of the gate-drain underlap. (b) Side view SEM image of a NW with gate-drain underlap fabricated with a SiO_2 spacer.

The DC transfer characteristics I_d-V_{gs} of a p-TFET and a n-TFET with suppressed ambipolar behavior are shown in Figure 3.26. The ambipolar behavior of both devices is completely suppressed even at large opposite V_{gs}. Both devices show

good subthreshold behavior with an average SS of 130mV/dec and 79.6mV/dec over 4 orders of drain current for the p-TFET and the n-TFET, respectively. SS shows a clear improvement compared to the devices shown by Luong. et al[23] with suppressed ambipolar behavior using NW array TFET concept achieving 139mV/dec in 3 orders of drain current. The p-TFET achieves on-current $I_{on} = 0.11\ \mu A/\mu m$ and n-TFET I_{on}= 0.28 $\mu A/\mu m$ at $V_{DD} = 0.5$V. According to these values a reduction in I_{on} current can be inferred. We believe that this reduction is caused by the intrinsic silicon layer in th gate-drain underlap. This region of our device is around 150nm in length, which contributes greatly to this reduction. according to reference [23] it can be concluded experimentally that shorter gate-drain underlap would allow higher currents. However, a very short underlap does not totally suppress the ambipolar behavior. Depending on the application and requirements, an optimum underlap length should be chosen.

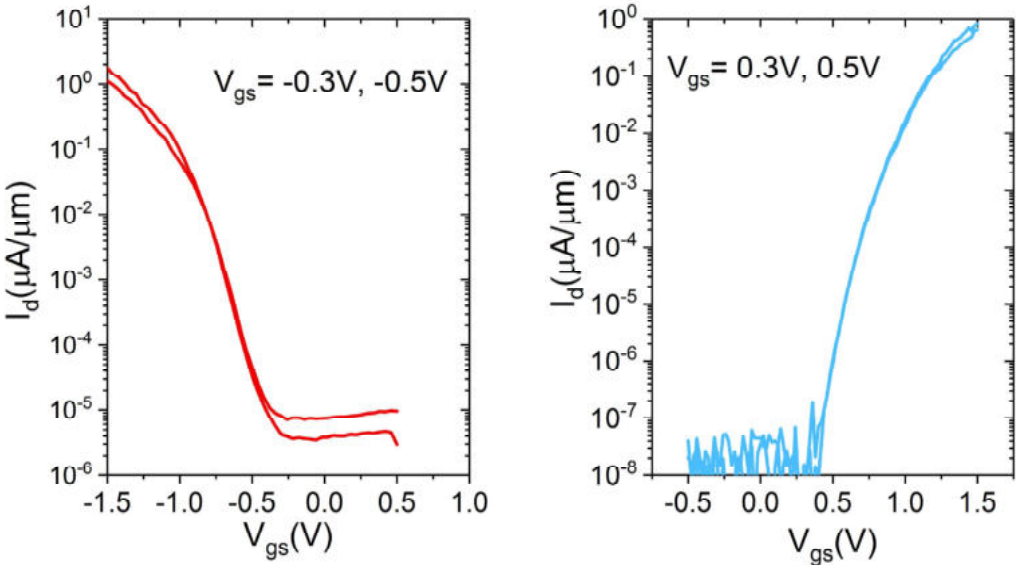


Figure 3.26: DC transfer characteristics I_d-V_{gs} for (a) p-TFET and (b) n-TFET with suppressed ambipolar behavior.

The corresponding output characteristics I_d-V_{ds} for the p-TFET and the n-TFET with suppressed ambipolar behavior were also recorded as shown in Figure 3.27. Both

transfer curves exhibit good saturation which is important for circuit applications. Moreover, there is no super-linear onset in the output of the nTFET indicating optimum doping concentration at its source.

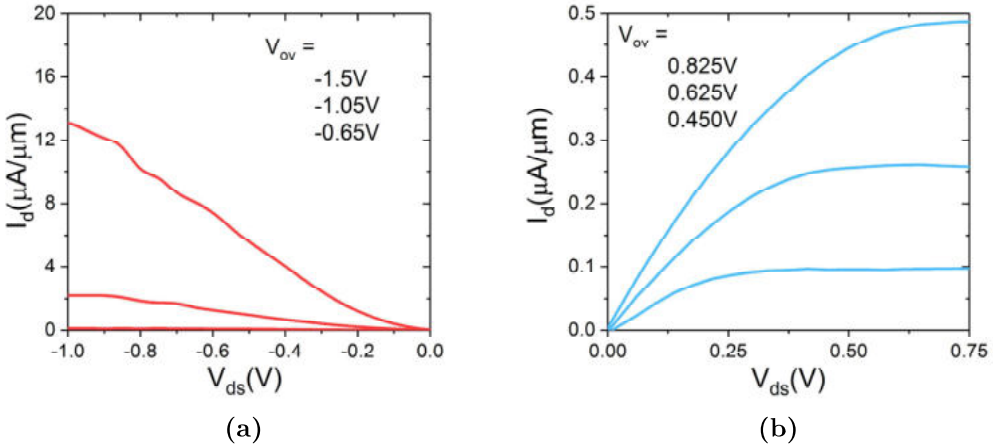


Figure 3.27: DC output characteristics I_d-V_{ds} for both (a)p-TFET and (b)n-TFET with suppressed ambipolar behavior.

3.7 Conclusion

In this chapter, single NW sSi TFETs were successfully fabricated and optimized to achieve maximum currents while keeping the average subthreshold slope low. We managed to evaluate effects of different process parameters, especially ion implantation and activation steps, to allow a comparison between resulting devices. The optimized n-TFETs delivered high on-currents of $15\mu A/\mu m$ at $V_{dd} = 0.5$V and a low average slope of 76mV/dec over 4 decades of drain current. Moreover, the analogue characteristics of the nanowire nTFETs were calculated to demonstrate its suitability for analogue circuit application. Furthermore, temperature and charge pumping measurements revealed the effects of TAT on the device performance, concluding that any future work has to address this issue with novel approach. Lastly, the fabrication and characterization of a method to systematically suppress the ambipolar behavior of both n- and p-TFET using gate-drain underlap was discussed.

Chapter 4

Complementary sSi single NW TFET based logic inverters

Due to their potentially lower power consumption, by providing low I_{off} and sharp transition to sufficient I_{on} current, TFETs are good candidates to replace MOSFETs for certain IC applications. In this chapter, our goal is to demonstrate inverters based on TFETs as basic building blocks of digital circuits. There are some challenges in achieving this goal due to the working principle of TFETs. Firstly, the ambipolar behavior of TFETs negatively affects inverters by reducing the noise margin. Secondly, both n-TFET and p-TFET should be simultaneously optimized and integrated on the same chip. It is important that both transistors get optimized and without super-linear onset in the device output characteristics, as it affects the noise margin of the circuit. Logic circuits based on TFETs have already been studied, for example: Trigate silicon C-TFET inverters with ambipolarity, silicon GAA NW p-TFET as p-logic NAND gate with ambipolar behavior. Here we show logic inverters by fabricating both n- and p-TFET on the same chip using single silicon NW GAA technology. To mitigate the effect of ambipolarity, we investigate two different methods namely asymmetrical doping and gate-drain under-lap, to suppress this undersitable feature. Moreover, we will study how the logic circuit functions at high temperatures.

4.1 Complementary MOS logic inverter

Complementary MOS(CMOS) inverter is the elementary unit of digital circuit design. The CMOS inverter comprises of an n-MOS and a p-MOS as shown in Figure 4.1, where V_{dd} is the supply voltage connected to the source of p-MOS, V_{in} is the input voltage shared on the gate of both devices and V_{out} is the output voltage of the inverter connected to the shared drain contact of the transistors, and finally source

of n-MOS is connected to the ground. When there is a high voltage on the input, the p-MOS will be off while the n-MOS will be in the saturation region creating a direct path between the ground and the V_{out} nodes. On the other hand, by decreasing the input voltage, the n-MOS will go into the cut-off region whereas the p-MOS is in the saturation region, creating a direct path between V_{dd} and V_{out} nodes. It should be noted that all the while in DC operation, input resistance of the CMOS inverter is very high considering that gate conducts little current in the steady state.

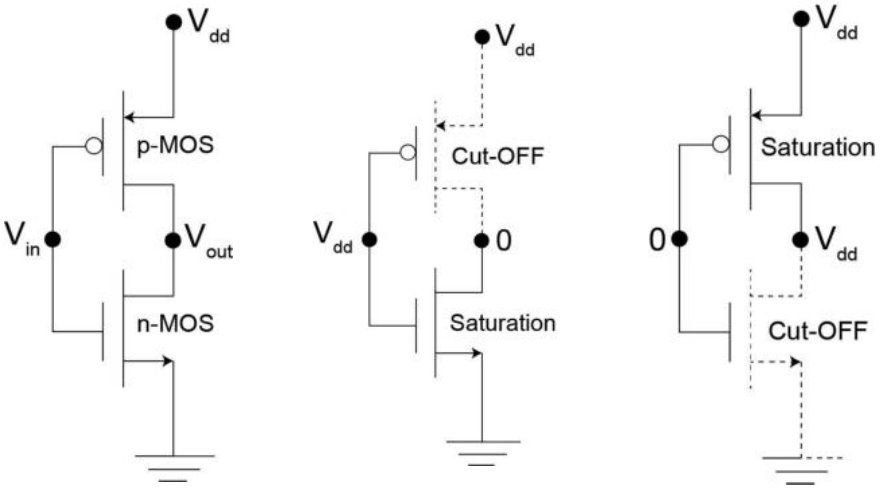


Figure 4.1: Schematics of Complementary MOS inverter as well as high-input and low-input circuits. V_{in} is connected to the gate and V_{dd} is the supply voltage.

4.1.1 Voltage Transfer Characteristics (VTC)

Voltage Transfer Characteristics (VTC) graphically represents the relation between the input voltage V_{in} and the output V_{out} of an inverter. It is the figure of merit for behavior of an inverter in DC operation. To deduce VTC graphically, one should super impose output characteristics of the n-MOS and p-MOS on each other to achieve the conventional load-line plot. In order to achieve this goal, drain current of the p-MOS is inverted since I_{d_n} = -I_{d_p}. Moreover, according to the relation $V_{ds_p} = V_{out}$ - V_{dd}, the x-axis of the p-MOS output characteristics must be shifted by V_{ds_p} + V_{dd} as shown in Figure 4.2(b). Hereafter one should find the points where current I_{d_n} meets I_{d_p}. In other words, each point should be located at the intersection of reciprocal lines for

the same V_{in} voltage. A number of these points are marked by distinct colors in the Figure 4.2(a) and (b) on the n-MOS and p-MOS output characteristics.

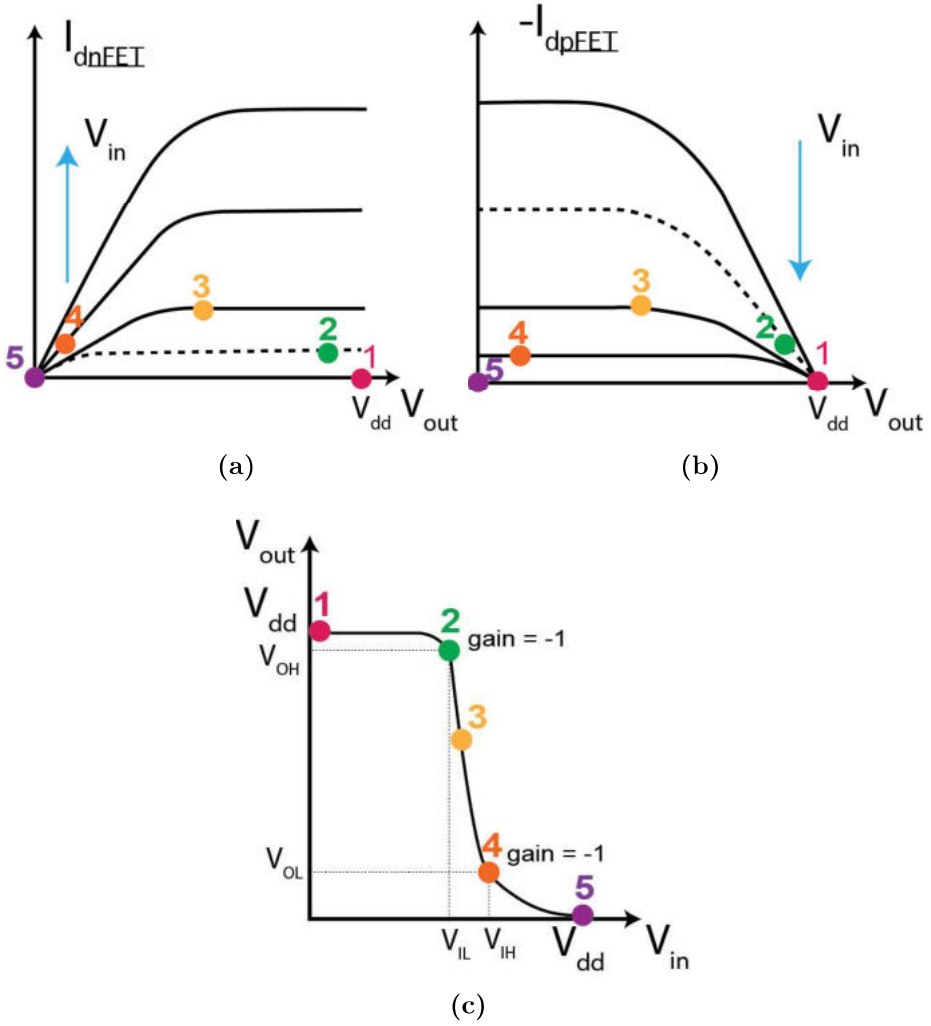


Figure 4.2: (a) Inversion of I_{dp} and shifting the x-axis of p-MOS output characteristics. (b) n-MOS output characteristics. (c) Corresponding load-line plot by super imposing n and p-MOS output curves. At each marked point both devices have the same current at a specific V_{in} voltage.

By plotting each point from the load-line against the reciprocal V_{out}, VTC curve is created, as shown in Figure 4.2(c). When n-MOS is off and p-MOS is in saturation region, $V_{out} = V_{dd}$, but when n-MOS is in saturation and p-MOS is off $V_{out} = 0$V. When both transistors go into the saturation , VTC flips, where in the case of matched

transistors, $V_{in} = V_{out} = V_{dd}/2$ is called the switching threshold and both devices at this point are in the in saturation region. In this case VTC is symmetric and has maximum noise margin. This point of switching threshold is referred to as V_M.

Noise margin

In an ideal inverter, a logic level is constant until $V_{in} = V_M = V_{dd}/2$ when it abruptly flips to the other logic level, like a step function. In other words, ideal inverter returns the desired constant output even in presence of considerable signal distortion or noise over the maximum range of $V_{dd}/2$. For a real inverter, however, the change is gradual and the input signal corresponds to the desired output only in a specified range before flipping, which this range is called noise margin(NM). The noise margin can be quantified for both high NM_H and low NM_L input states. To approximate NMs, we first calculate the points in VTC at which the inverter gain is equal to $gain = \frac{dV_{out}}{dV_{in}} = -1$. Each of these points correspond to operational point pairs (V_{IH}, V_{OL}) and (V_{OH},V_{IL}) which are marked in Figure 4.2(c). According to these definitions, noise margins can be defined as:

$$NM_L = V_{IL} - V_{OL} \tag{4.1}$$

$$NM_H = V_{OH} - V_{IH} \tag{4.2}$$

A simpler approach to calculate NM_L and NM_H is by using the so-called piecewise linear approximation for the VTC. In this method, it is assumed that $V_{OH} = V_{dd}$ and $V_{OL} = 0$. Moreover, a straight line through V_M point with a slope of $g = gain_{V_M}$ is plotted. The intersection of this line with V_{OH} and V_{OL} lines give V_{IL} and V_{IH} respectively. By having these values noise margins relations are as:

$$NM_L = V_{IL} \tag{4.3}$$

$$NM_H = V_{DD} - V_{IH} \tag{4.4}$$

Looking at these relations it is obvious that to achieve the maximum noise margin the transition region should be as small as possible with highest gain.

4.2 Single NW sSi GAA CTFET inverters

In order to fabricate the inverter with p-TFET and n-TFET on the same mesa, a similar approach to the fabrication steps in Section 3.2 was taken. Two single nanowire TFETs, as shown in Figure 4.3, were fabricated on a sSOI substrate sharing their drain contact directly via mesa. Moreover, to suppress the ambipolar behavior for the p-TFET, we took advantage of asymmetric doping of source and drain. So the p-TFET source was implanted with higher dose of phosphorous compared to boron at its drain. It should be noted that for each step of implantation specific windows by e-beam resist was opened leading to a total of 4 ion implantation steps. However, the activation step was carried out in a single step at 600°C by RTP. The reason for higher activation temperature was to reduce possible implantation damage for subsequent temperature characterization of the inverter. As gate stack 3nm ALD HfO_2, along 60nm AVD TiN for good coverage of nanowire and maintenance of oxide quality, were deposited and patterned. As shown in Figure 4.3, supply voltage V_{dd} is connected to p-TFET source while n-TFET source is grounded. The gate contact acts as V_{in} connected to both transistors simultaneously.

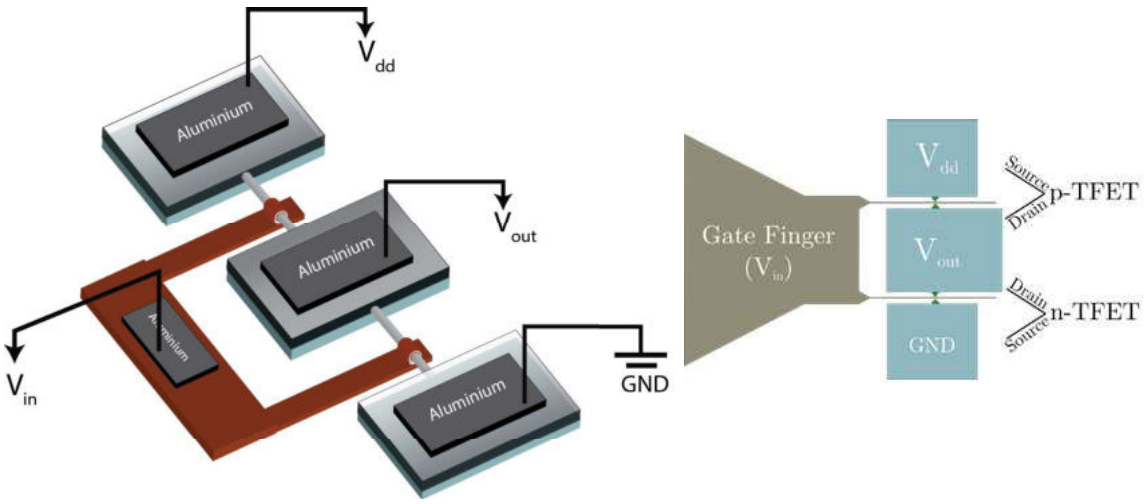


Figure 4.3: Schematics of single NW sSi GAA CTFET inverter with both transistors on the same mesa. Source and drain of n-TFET and p-TFET and their corresponding bias mode is specified.

4.2.1 Individual device characteristics

We will start by characterizing each device individually. The transfer characteristics of p- and n-TFET are shown in Figure 4.4. Both devices show similar current levels at matched V_{ov} voltages. As it is apparent, the asymmetric doping of p-TFET was successful at suppressing the ambipolar behavior for this device, thus potentially improving NM_H of the inverter. On the other hand, n-TFET still shows strong ambipolar branch in its off state, which is detrimental to NM_L and gain of the inverter at room temperature. Both devices show unoptimal subthreshold slope SS which is in expected from the relatively high activation temperature of 600°C. Another important parameter to consider is the difference between onset voltage of the devices $V_{p_{onset}}$ - $V_{n_{onset}}$ = 0.87V meaning that to saturate both devices large range of input voltage is required and thus limiting V_{dd} reduction for the inverter.

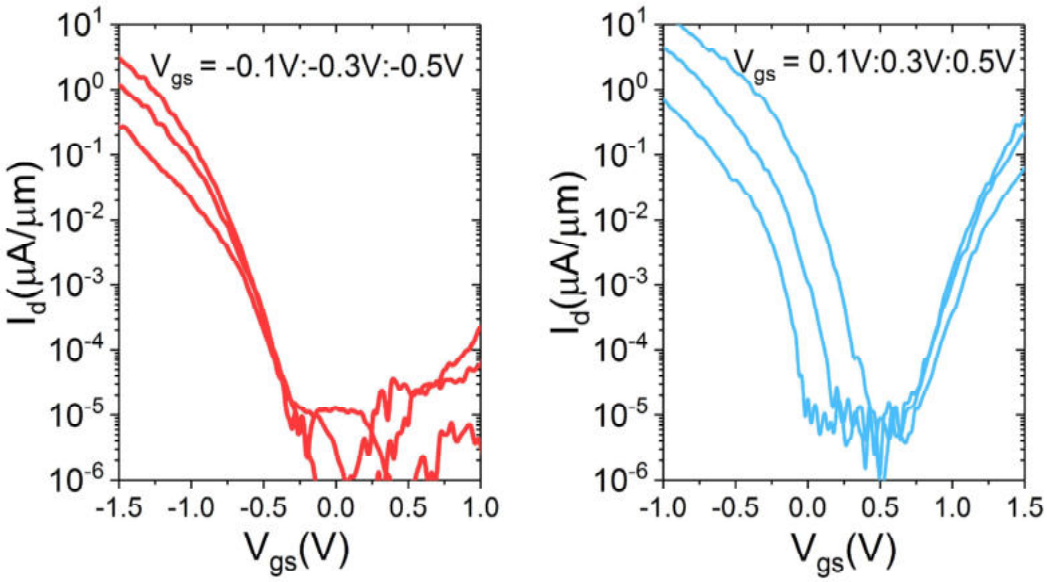


Figure 4.4: Individual transfer characteristics of p-TFET(a) and n-TFET(b) for different V_{ds} fabricated on the same mesa to act as an C-TFET inverter. The ambipolar behavior of the p-TFET is effectively suppressed due to the asymmetric doping.

For each individual device the output characteristics I_d vs V_{ds} are shown in Fig-

ure 4.5 based on V_{ov} = V_{gs} - V_{off}, where I_{off} = $1nA/\mu m$. Due to high activation temperature the dopant concentration is not high enough to prevent tunneling distance change by sweeping V_d, hence the super linear onset is present.

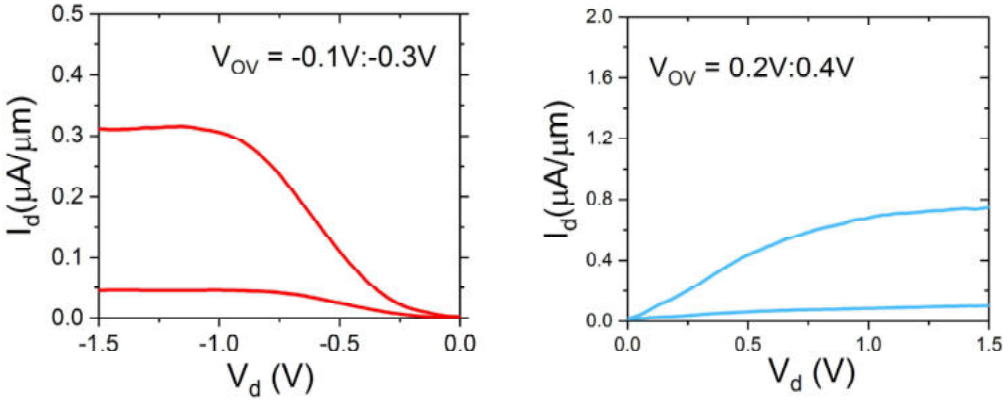
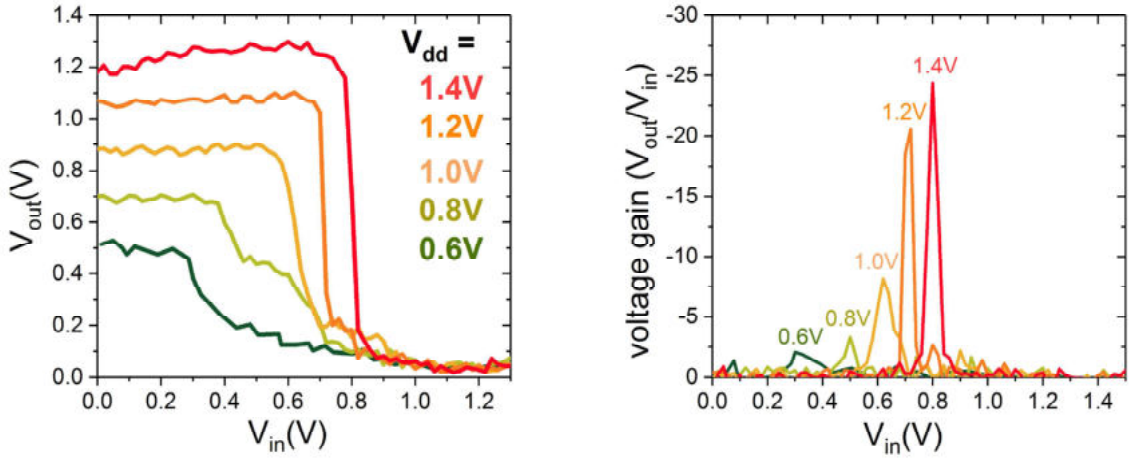


Figure 4.5: Individual output characteristics I_d-V_{ds} of p-TFET(a) and n-TFET(b) for different V_{ov} fabricated on the same mesa to act as an C-TFET inverter.

4.2.2 Inverter VTC at room temperature

The voltage transfer characteristics(VTC) of the inverter with sSi single GAA NW CTFET was measured for bias points from V_{dd} = 1.5V down to 0.6V, as shown in Figure 4.6(a). Two distinct behaviors are recorded for the low and high input voltage V_{in}. In the case of low V_{in}, the output V_{out} does not reach the respective bias point voltage and moreover tends to decrease by decreasing V_{in}. Whereas, at high V_{in}, beyond the VTC flipping point, the V_{out} values are much closer to the GND and are constant over a wide range indicating good noise margin. This stems from the fact that in the former case, when the p-TFET is on, the ambipolar branch of n-TFET is conducting, hindering V_{out} from reaching V_{dd}. By decreasing V_{in}, V_{gs_n} gets more negative, giving rise to stronger ambipolar branch and consequently further decreasing V_{out}. As a consequence, for smaller V_{dd}, this effect is more pronounced being more susceptible to the interference. On the other hand, since the ambipolar branch of p-TFET was suppressed by the asymmetric doping of source and drain,



(a) (b)

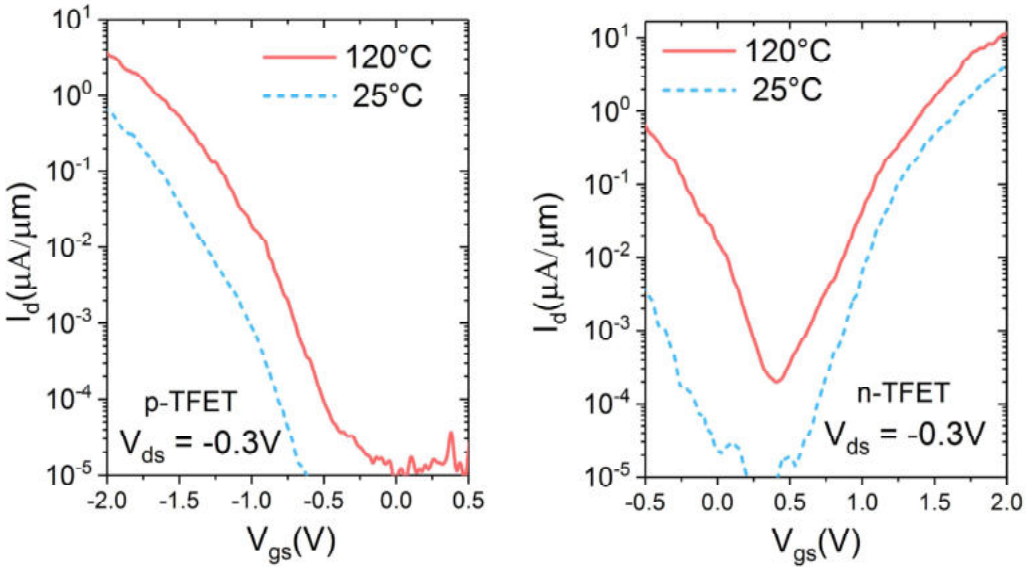
Figure 4.6: Room-temperature measurement of single NW GAA c-TFET inverter. (a) Voltage transfer characteristics(VTC).(b) Corresponding voltage gain of VTC, dV_{out}/dV_{in}.

good noise margins are achieved. The switching threshold V_M of VTC is shifted to the right by almost 0.1V. This is caused by the asymmetric characteristics of the inverter. For example, for V_{dd} = 1.4V, at $V_{dd}/2$ = 0.7V, n-TFET current is still too small for saturation, hence the V_M is shifted to 0.8V. At V_{dd} = 1.4V noise margins are NM_L =0.54V and NM_H =0.74V, however, NM_L never reaches the actual V_{dd} level. Inverter gain was calculated for corresponding voltages as shown in Figure 4.6(b). The inverter achieves maximum gain of 25 at V_{dd} = 1.4V and around 3 for V_{dd} = 0.6V.

4.2.3 Inverter operating at elevated temperature

An inverter fabricated with the method described in Section 4.2 was measured at room temperature and 120°C to evaluate its high temperature behavior. Figure 4.7 depicts the corresponding individual DC transfer characteristics I_d-V_{gs} for both n-TFET and p-TFET devices. The devices show on-set difference $\Delta V_{onset_{25}}$ of 1.32V at room temperature while at 120°C $\Delta V_{onset_{120}}$ = 0.8 is recorded and characteristics have become more symmetric. On-currents of both devices are increased due to dependence

of band-gap E_g on temperature. Moreover, due to presence of non-idealities, especially trap assisted tunneling, the subthreshold slope SS is degraded and I_{off} is increased at the elevated temperature. I_{on} current of n-TFET at room temperature for (V_{ds} = 1V, V_{gs} = 1.4V and 1.6V) is $0.71\mu A/\mu m$ and $2.87\mu A/\mu m$ while at 120°C its I_{on} at (V_{ds} = 1V, V_{gs} = 1.2V and 1.4V) is $0.6\mu A/\mu m$ and $2.80\mu A/\mu m$, respectively. As it is apparent, the effect of the elevated temperature on I_{on} is equal to an increase of 0.2V in V_{gs}.



(a) (b)

Figure 4.7: High temperature measurement of DC transfer characteristics I_d-V_{gs} for both (a)p-TFET and (b)n-TFET devices.

The output characteristics I_d- V_{ds} for both temperatures are shown in Figure 4.8. Apart from the increase in current, it is more remarkable that the p-TFET shows more distinct super-linear onset, both, at room and elevated temperatures in comparison to the n-TFET. This can potentially degrade switching performance of the inverter at low V_{in} voltage.

Voltage transfer characteristics of the inverters were recorded for V_{dd} = 1.4V at room temperature and 120°C as shown in Figure 4.9(a). The switching threshold voltage V_M has changed from 0.6V to near $V_{dd}/2$ at 0.7V at higher temperature,

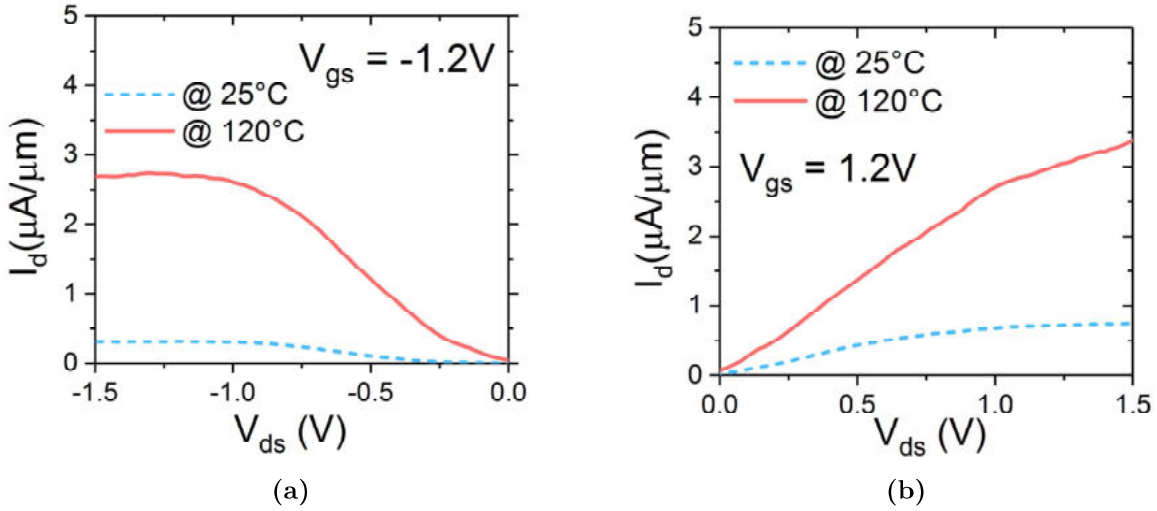


Figure 4.8: Output characteristic I_d-V_{ds} for both (a) p-TFET and (b) n-TFET devices at room temperature and 120°C.

because the characteristics have become more symmetric. At high V_{in}, the output voltages is almost pulled down to zero giving rise to good noise margin. This is as expected, since the ambipolar behavior of the pTFET is suppressed by asymmetric doping. At low V_{in}, due to the positioning of the ambipolar curve, it exerts less current at a given voltage when p-TFET pulls V_{out} to V_{dd}, causing logic behavior to match the actual bias point. This corresponds to the finding of Luong et al[87] that by changing gate work function to adjust the ambipolar curve, it is possible to suppress its negative effect in the inverter operation. Moreover, the voltage gain has improved more than two times from 18.7 to 44.2 by increasing temperature. For lower bias voltages than $V_{dd} = 1.4$V, the output characteristics of the individual devices deteriorated rapidly by increasing temperature, severely impacting the inverter VTC. This means that as long as TFET operates at a bias point, where the thermionic processes like TAT are not significant, can perform pretty good at elevated temperatures.

4.3 GAA CTFET inverter with suppressed ambipolarity

Single sSi GAA NW TFETs with suppressed ambipolar behavior using drain-gate underlap were fabricated, according to the process discussed in Chapter 3. N-TFET

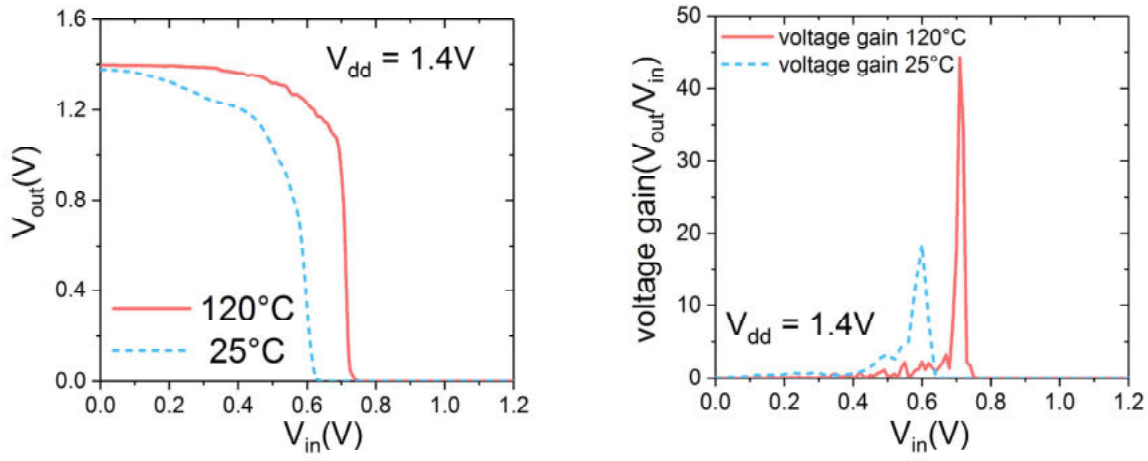


Figure 4.9: High temperature measurement of a single NW GAA c-TFET inverter at 120°C. (a) Voltage transfer characteristics(VTC).(b) Extracted voltage gain dV_{out}/dV_{in}

and p-TFET devices were integrated to form an inverter where Figure 4.10 shows the transfer characteristics I_d-V_{gs} of the devices at V_{ds} = -0.5V. Both devices show suppressed ambipolar behavior even at high opposite V_{gs} voltages. However, due to the long intrinsic region between gate and drain the current level is rather decreased. Moreover, there is a relatively high 1.2V difference between onset voltages of both devices. This means that relatively high V_{dd} is required for saturation of both transistors, as needed for functioning of the inverter. Moreover, the characteristics are not symmetric around zero volt and are shifted to the right, which will result in a shift of V_M to the right. It should also be noted that for voltages in the subthreshold region, gate leakage of the p-TFET is comparable to I_d of the n-TEFT. Hence, this leakage current could act as a virtual ambipolar behavior, degrading the inverter.

The inverter VTC was recorded for V_{dd} = 2V down to 1.5V(Figure 4.11(a)), where switching threshold V_M is shifted to the right of $V_{dd}/2$ at a small voltage, stemming from the fact that transfer characteristics are not symmetric around 0V. The VTC shows that for V_{dd} = 1.7V and 2.0V the effect of ambipolar behavior is completely suppressed. This means that the V_{out} logic levels match the respective high(V_{dd}) and low(GND) voltages almost perfectly. For V_{dd} = 1.4V and 1.1V there is a region of

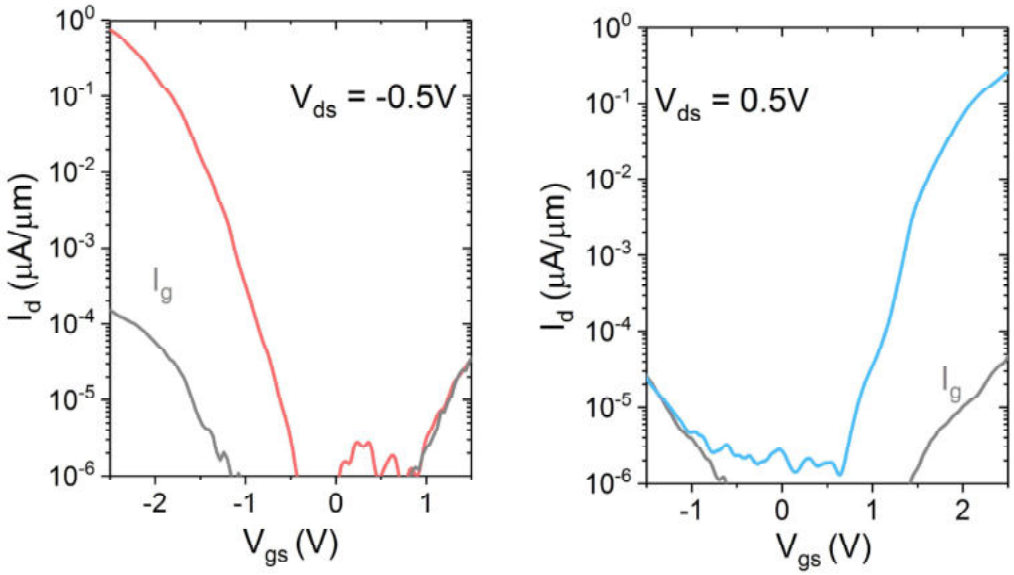


Figure 4.10: Transfer charactersitics I_d -V_{gs} for (a) p-TFET and (b) n-TFET, with suppressed ambipolarity using gate-drain underlap, integrated on the same mesa for logic inverter measurement, as explained in Figure 4.3.

V_{in_H} where V_{out} first saturates at a higher voltage than GND and then drops down gradually to 0V. For example in case of $V_{dd} = 1.1$V, this region is located between 0.7V to 1V of the input voltage. This region corresponds to the V_{gs} voltages where gate leakage current of the p-TFET is comparable to I_d of the n-TFET, thus acting like a virtual ambipolar behavior. One way to go around this issue is to adjust the threshold voltage of the devices by using different gate material for them. Figure 4.11(b) shows the VTC voltage gain. Voltage gain is not very high, even at $V_{dd} = 2$V it equals to 15, which is much less in comparison to the inverter in section 4.2 with gain of 24 at $V_{dd} = 1.5$V. This is because transition from saturation region to linear region is not sharp enough and should be improved by optimizing the devices. Noise margin was calculated for $V_{dd} = 2.0V$ as $NM_L = 0.95V$ and $NM_H = 0.85V$ amounting to about 47.5% and 42.5% of the applied V_{dd} respectively.

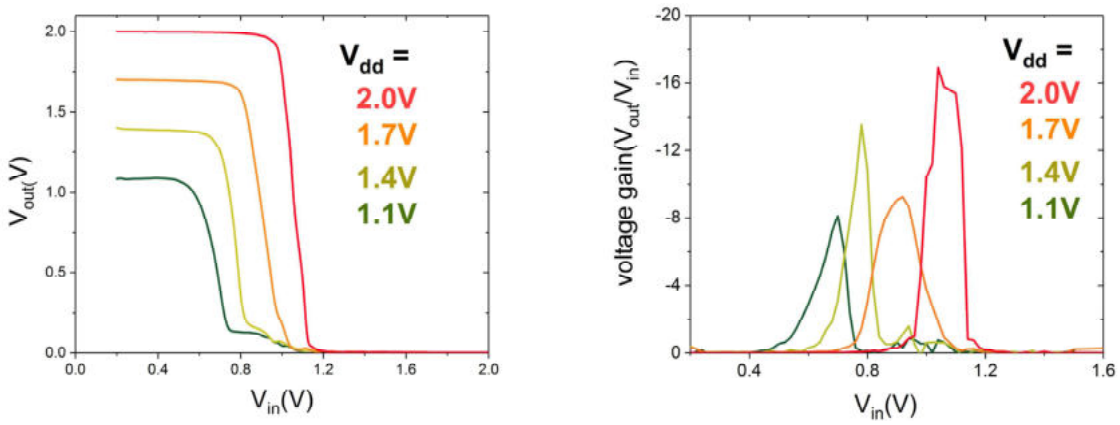


Figure 4.11: Single NW GAA C-TFET inverter with suppressed ambipolar behavior. (a) Voltage transfer characteristics.(b) Corresponding voltage gain of VTC.

4.4 Conclusion

In this chapter we have presented the results of fabrication and characterization of static behavior of complementary TFET inverters based on silicon single nanowire devices. Two different types of inverters were fabricated. In the first type, the ambipolar behavior of the pTFET was suppressed by asymmetric doping of source and drain. The second type of inverter was fabricated using n- and p-TFETs with suppressed of ambipolarity using gate-drain underlap. The VTC of the first type of inverter achieved better NM_H than NM_L due to the suppression of the pTFET ambipolarity. The inverter showed a voltage gain of over 25 at $V_{dd} = 1.4$V. Moreover, it was shown that increasing temperature can enhance the inverter behavior at certain bias points. For example, at $V_{dd} = 1.4$V, the inverter gain showed more than twice improvement at 140 compared to room temperature. This conclusion is not necessarily true for low voltages since by increasing temperature, the sub-threshold performance of TFET could degrade due to TAT. Lastly, the second type of inverter with suppressed ambipolarity was presented. The logic levels for this inverter perfectly matched the actual bias points, improving the noise margins considerably.

Chapter 5

Line-tunneling Silicon TFET

In this chapter, we investigate a novel approach to take advantage of line tunneling with source-gate overlap to improve the subthreshold slope and I_{on} of devices. Conventional point tunneling takes place at p-i or n-i junction, while in devices with source-gate overlap, provided with enough band bending, line tunneling occurs from the source to semiconductor-oxide interface (Figure 5.1(a),(b)). It has been shown that line-tunneling can achieve steeper SS [88]. However, in a real device both of these contributions are present as depicted in Figure 5.1(c).

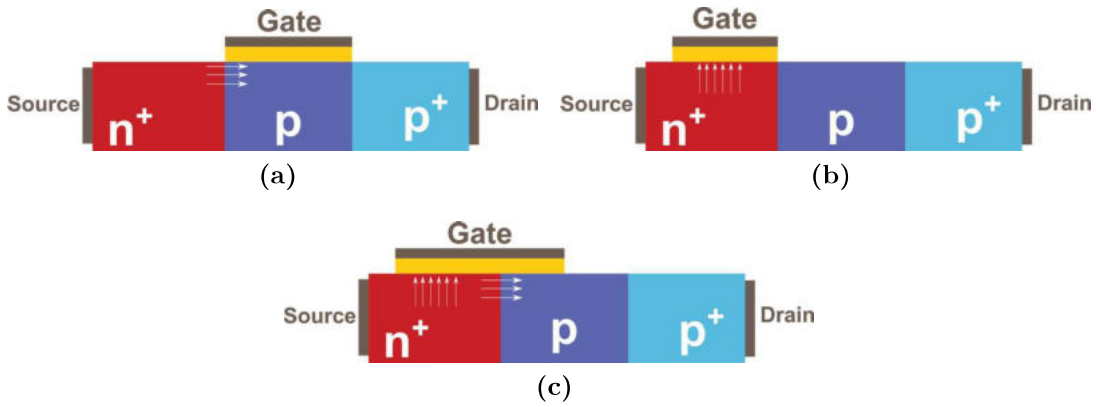
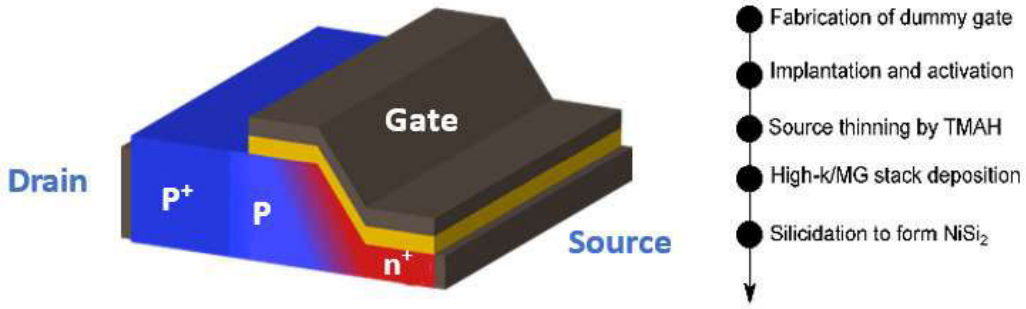


Figure 5.1: pTFET device configuration. (a) Tunneling path of carriers in case of point-tunneling, where tunneling occurs at the source channel interface. (b) Tunneling path of carriers in case of line-tunneling where the tunneling takes place in the gate/source overlapped region with a direction parallel to the gate electrical field. By applying a gate voltage a depletion/inversion region beneath the gate is formed and carriers tunnel to the oxide interface. (c) In a real device, both tunneling mechanisms contribute to the current.

5.1 Device fabrication

TFET devices as illustrated in Figure 5.2 were fabricated on normal 22nm SOI wafer with 145nm buried oxide as starting substrate. The fabrication concept is to first create junctions and then deposit the gate. Therefore, the process is not self-aligned and requires pattern alignment at each step.



(a)

Figure 5.2: Device schematics and key fabrication process steps. After implantation and activation, the source is thinned down through wet etching to get rid of EOR damages.

- The SOI wafer was cut into 19.5x19.5m^2 pieces and was cleaned by propanol and acetone solutions. Samples were further cleaned in piranha solution H_2SO_4:H_2O 2:1 for 5 minutes to remove any possible organic contamination on the surface.
- 80nm PECVD SiO_2 was deposited in order to prepare structure for implantation. Then it was patterned and dry etched in CHF_3 plasma to open the implantation window. After this step the resist was stripped away in acetone. Consequently, the samples were dipped in 1 percent HF for 15 seconds to remove possible oxide residuals. This process was carried out for each individual implantation steps intended for source and drain junctions.
- The implantation was carried out with boron for drain and phosphorous for source at zero tilt, while energy and dose were carefully selected based on simulations. Phosphorous was implanted with two different implantation doses of 2x10^{14}cm^{-2} and 2x10^{15}cm^{-2} to compare resulting devices. TRIM simulation of implantation for phosphorous in Figure 5.3(a) shows that EOR damages reside

at around 10nm depth, indicating the importance of thinning down the source area to less than 10nm. After the implantation, rest of SiO_2 was removed to prepare samples for next implantation steps.

- When both implantation steps were carried out, dopants were activated using spike annealing at 1050°C. We used spike annealing to recover as much implantation damage as possible and also to get a homogeneous doping profile over the depth of the SOI. To perform spike annealing, first temperature is stabilized at 625°C for 105 seconds in N_2 environment. Then with rate a of 50 °C/s it is increased to 650°C. After 10 seconds with rate of 250 °C/s it is increased to 1050°C and held at this temperature for 2 seconds before cooling down with rate of -250 °C/s. The TCAD simulated dopant profile after annealing (Figure 5.3(b)) further indicates an active dopant concentration of $3x10^{19}cm^{-3}$ for a dose of $2x10^{14}cm^{-2}$ at a depth of 15nm, corresponding to a source thickness of 5nm after thinning down as described below.

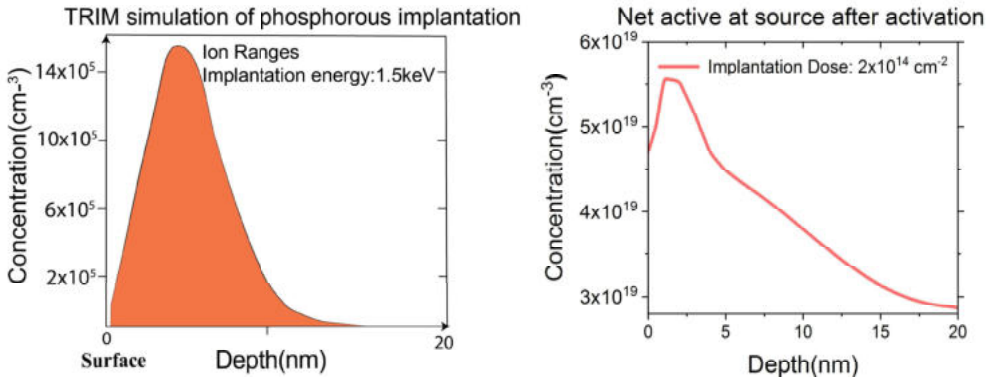


Figure 5.3: (a) TRIM simulation of the implantation. Point of maximum damage and EOR region are marked in the plot. (b) Net active dopant concentration achieved using Sentaurus TCAD process simulation for implantation and subsequent spike annealing at 1050°C.

- After annealing, the oxide was removed in HF and 60nm PECVD SiO_2 was deposited and patterned to open a window for thinning down the source junction. Source was etched down to 5nm at room temperature by wet etching in TMAH solution.

- 3nm of ALD HfO_2 and 60nm of PVD TiN were deposited and patterned to form the High-k/Metal Gate stack. 2nm of Ni was deposited and annealed at 750°C for 30 seconds to form $NiSi_2$ with smooth interface and low resistivity[89].
- passivation and Al metalization.

5.2 Device characterization

Figure 5.4(a) depicts the I_d-V_{gs} transfer characteristics of the fabricated pTFET device with $2\mu m$ channel length and $2\mu m$ gate width. The source of the device was ion implanted by phosphorus at 1.5keV energy and dose of $3x10^{14}cm^{-2}$. After activation, it corresponds to a dopant concentration of $3x10^{19}cm^{-3}$ at 5nm silicon thickness based on process simulations. Thenceforth we name this device T1. The device T1 shows steep increase of current with an average SS of 55mV/dec over two decades of I_d current between $1.5x10^{-13}$ to $1.5x10^{-11}$ $\mu A/\mu m$ at V_d = -0.1. Furthermore, the I_{on} /I_{off} ratio is about $2.55x10^2$ at $V_{ds} = V_{on} = V_{gs}$ -V_{off} = -0.5V for I_{off} = 1nA/µm. However, with this definition of I_{off}, the steepest part of the characteristics is neglected. If we take $I_{off} = I_{onset} = 1x10^{-13}$, V_{on} = -0.5 and V_{ds} = -0.1V, then $I_{on}/I_{off} = 6.4x10^5$ which is pretty remarkable.

A hump is present in the SS vs I_d plot as shown in Figure 5.4(b). It divides the transfer curve to two distinct regions at a current of about $0.5x10^{-10}$ $\mu A/\mu m$. In order to explain the existence of these two different regions, Figure 5.5 depicts different tunneling regions and mechanisms in our device. As shown, line-tunneling takes place in two distinct areas in the device. One region extends over the thinned source and the other region is located in the thick part. Due to the existence of the fringing fields at the thicker region, line-tunneling is particularly stronger in this region. Point tunneling is also present in the device but its contribution due to low dopant concentration at source-channel junction is negligible. To investigate these processes in detail, TCAD simulation with Sentaurus was carried out. In the simulation models for drift-diffusion transport, doping dependent SRH generation-recombination and non-local BTBT and fermi statistics has been considered for the structure and applied to solve the Poisson equation. Moreover, parameters for the high-k dielectric and silicon were taken from the standard library of the software. The main goal of the simulations is to help understand the different tunneling processes in the device. The simulated characteristics achieve lower current than what is measured

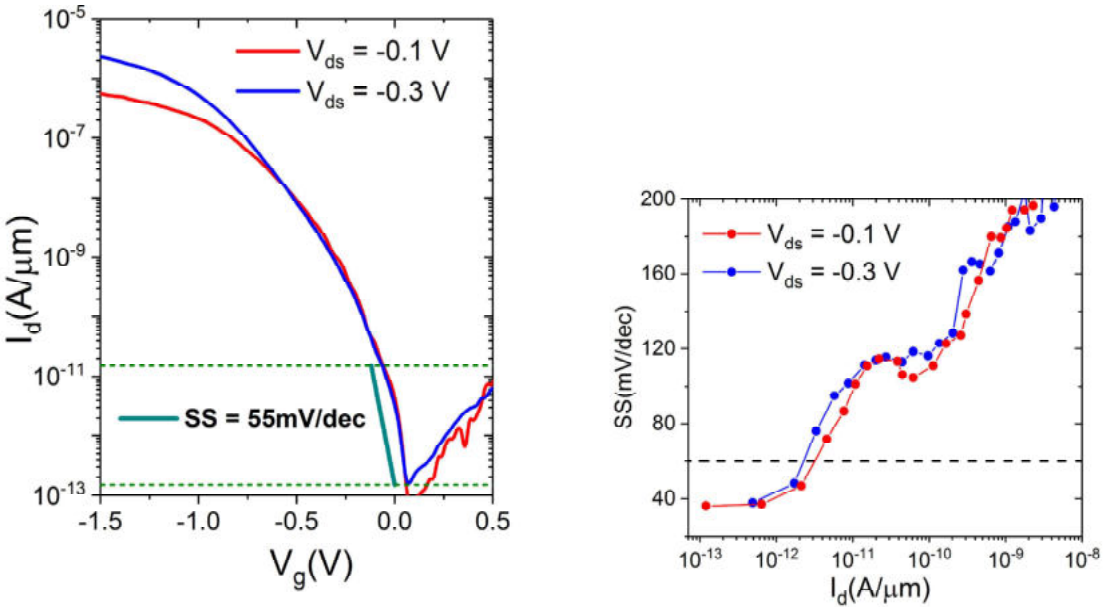
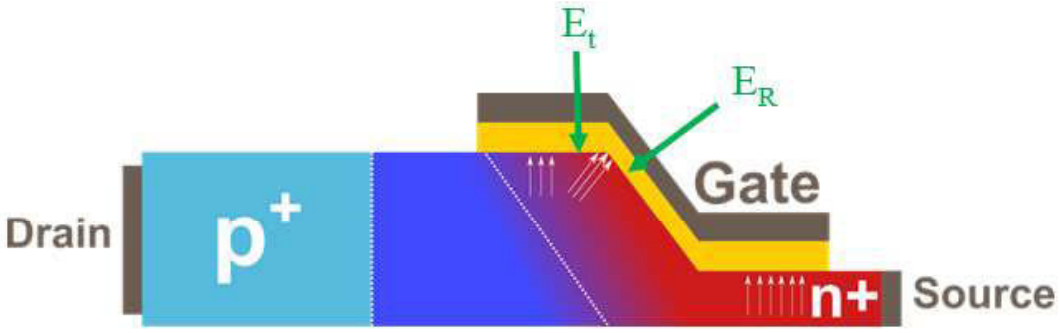


Figure 5.4: (a) DC Transfer characteristics I_d-V_{gs} of transistor T1 pTFET with lower source doping. (b) SS vs I_d plot of the transfer curve. The hump is caused by the different line-tunneling onset voltages in the top corner and in the thin source area.

experimentally. This difference is caused by other effect like TAT, band-gap-narrowing and non-calibrated models and parameters for such the device structure.

Figure 5.6(a) shows the simulated transfer characteristics of the device at V_d = -0.3V. At V_{gs} = -0.1V line-tunneling initially starts at the top corner as a result of fringing field induced tunneling and then extends on the ramp due to contribution of E_t and E_R as indicated in Figure 5.6(b). Increasing V_{gs} to -1V causes the line tunneling in the thinner area as shown by the contour of band to band generation in Figure 5.6(c). This further increases the current but gives rise to the hump in the characteristics.

Another device with a higher source implantation dose of 2×1015 cm-2 at 1.5keV energy was fabricated. The dc transfer characteristics I_d-V_{gs} of the device are shown in Figure 5.7(a). For the sake of easy referencing, this device is called T2. Since this device has higher doping concentration, the line-tunneling induced by the fringing field at the thick part of the device starts at an earlier voltage. This results in



(a)

Figure 5.5: Different tunneling mechanisms in the fabricated device are shown schematically. Line tunneling takes places in two distinct regions: one in the thin source area and the other on the surface of the thick part of the source. Since the top corner at thick part has a higher electric field due to the existing fringing fields, the tunneling is induced earlier at that point before extending over the ramp and in the end on the thin part of the source.

onset-voltage shift of 0.25V. It was shown by simulation that increasing the dopant concentration, improves the electric field at the corner of the thicker more strongly than the thin part of the source, as depicted in Figure 5.8. This higher electric field at the corner means an earlier onset for BTBT. It is important to note that the electric field in the top corner shows higher change with doping concentration in comparison to the electric field in the flat thin source. On the other hand, a higher voltage V_{gs} is required to form a depletion region for line-tunneling at the thin area of the source in the device T2 owing to the higher doping concentration. This also creates a hump in the characteristics which is also clearly visible in SS vs I_d plot for transistor T2 in Figure 5.7(b). However, this hump occurs at a higher voltage compared to transistor T1, appearing at V_{gs} = -0.09V for T1 whereas it appears at higher voltage of V_{gs} =-0.21V for T2. As discussed due, this stems from the higher doping concentration.

The recorded output characteristics I_d-V_{ds} of the pTFET T1 is shown in Figure 5.9. It is shown for two overdrive voltages of $V_{ov} = V_g - V_{off}$ = -0.5V and -0.3V where $I_{off} = 1nA/\mu m$. For small V_d there is a minor super-linear onset. Verhulst et al [90] have shown that this behavior for line-tunneling is caused as shorter tunneling paths are made available, resulting in an exponential dependence of I_d on V_d.

To decrease the super-linear onset in the output characteristics, either a lower

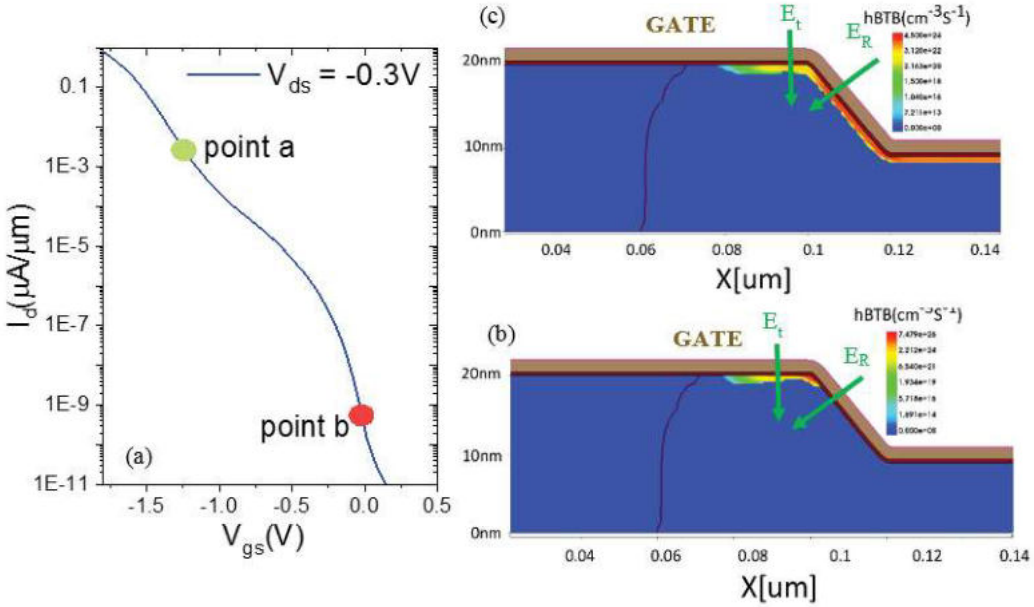
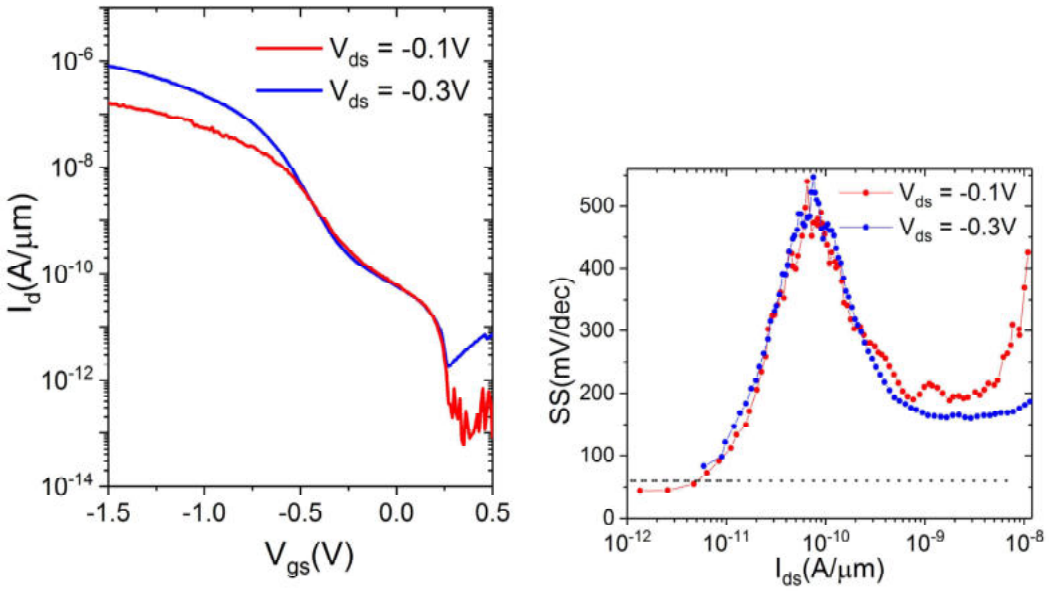


Figure 5.6: (a) Simulated transfer characteristics of the fabricated device at V_{ds} = -0.3V. (b), (c) show zoomed in contour of the device for different V_{gs}. Source is on the right side, while drain is on the left and gate extends all over the top section of the device. (b) Contour of BTB hole generation at V_{gs} = -0.1V shows that line-tunneling first occurs at the corner due to the high fringing field. (c) BTBT generation of carriers at V_{gs}= -1V shows that the hump in the characteristics is due to the late start of line-tunneling in the thinner area of source.

bandgap material or higher doping at the source junction is required. On the other hand, as mentioned before, a higher doping increases the onset voltage difference between the line-tunneling induced by the fringing field at the top corner and the tunneling at the thinned source. In this regard, a modification to structure is proposed to limit the doping to under the thin part of the source. This means getting rid of line-tunneling induced by the fringing fields at the top corner, as shown in Figure 5.10(a). Now only line-tunneling contribution from the thin source area is expected (Figure 5.10(b)). The simulated transfer characteristics of the proposed structure is shown in Figure 5.10(c). An ion implantation dose of 2x10^{14}cm^{-2} was considered at drain-source voltage was set to V_d = -0.1V. The proposed device does not show the hump anymore and has a much steeper subthreshold slope SS.



(a) (b)

Figure 5.7: (a) Measured transfer characteristics of a pTFET device with higher source doping. Notice the obvious shoulder in the curve, which is caused by stronger fringing field and starts earlier than line-tunneling at the thin part. (b) SS vs Id plot shows the effect of the bump more clearly.

5.3 Back gate bias effects

Since the device is fabricated on an SOI wafer, the effect of a second gate on the characteristics was studied by treating the buried oxide and back of the wafer as a back gate for the transistor.

The back gate was biased with three different voltages of V_{bg} = -10V, 0V, 10V at V_d = -0.3V. The transistor had a doping similar to the device T1 shown in Figure 5.4. The transfer characteristics as well as SS vs I_d plots of the measured device are presented in Figure 5.11. It is observed that a positive V_{bg} decreases I_{on} and degrades SS, while by applying a negative V_{bg}, minimum SS improves and I_{on} enhances. The improvement in SS shows some points under 60mV/dec. It is worth mentioning that the back gate gate covers all the area from the source to channel to drain. As a result, the electric fields of the back gate bias affects the the depletion region in the drain as well as the source. When a negative V_{bg} is applied, an additional depletion

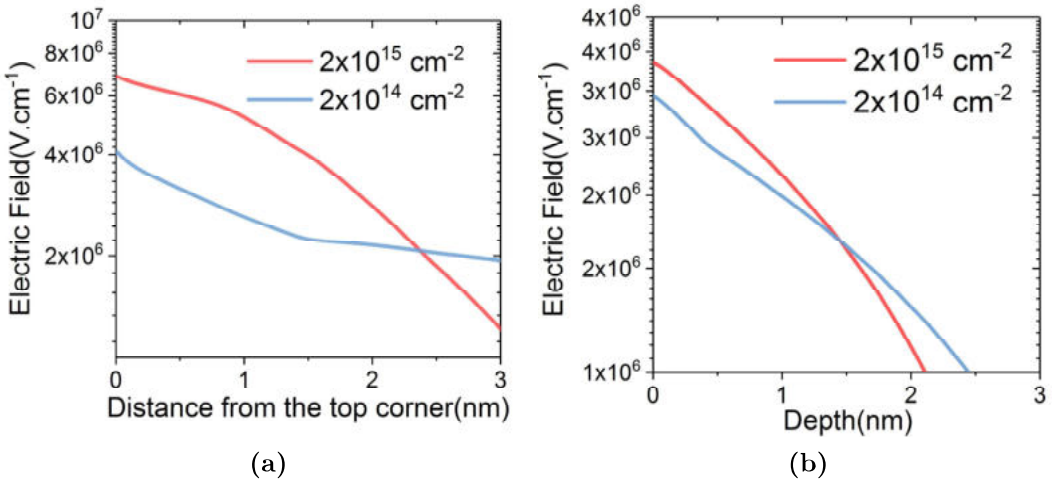


Figure 5.8: Simulated electric field in the device for two different implantation doses. (a) In the diagonal direction from the top corner. (b) Normal to the thin part of the source surface.

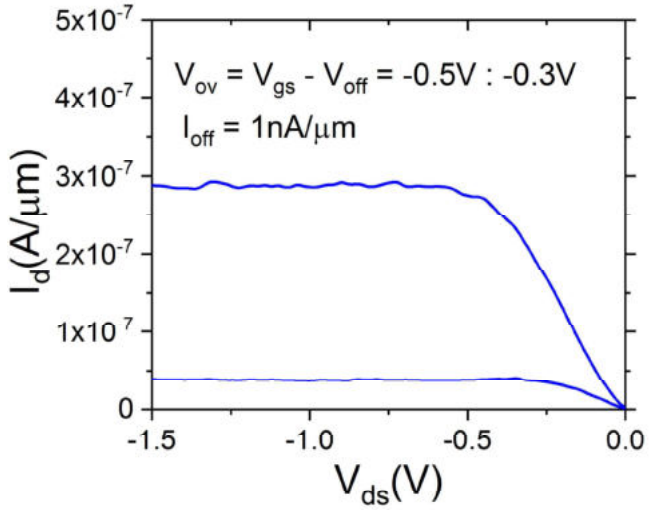


Figure 5.9: DC output characteristics I_d-V_{ds} of device T1 showing very good saturation and slightly super-linear behavior at small drain-source voltages.

region on the source side of the device near the back gate is created which contributes to the overall current. This leads to the higher recorded I_{on} current and improved SS. This extra contribution is mainly caused by the thick part of the source as an

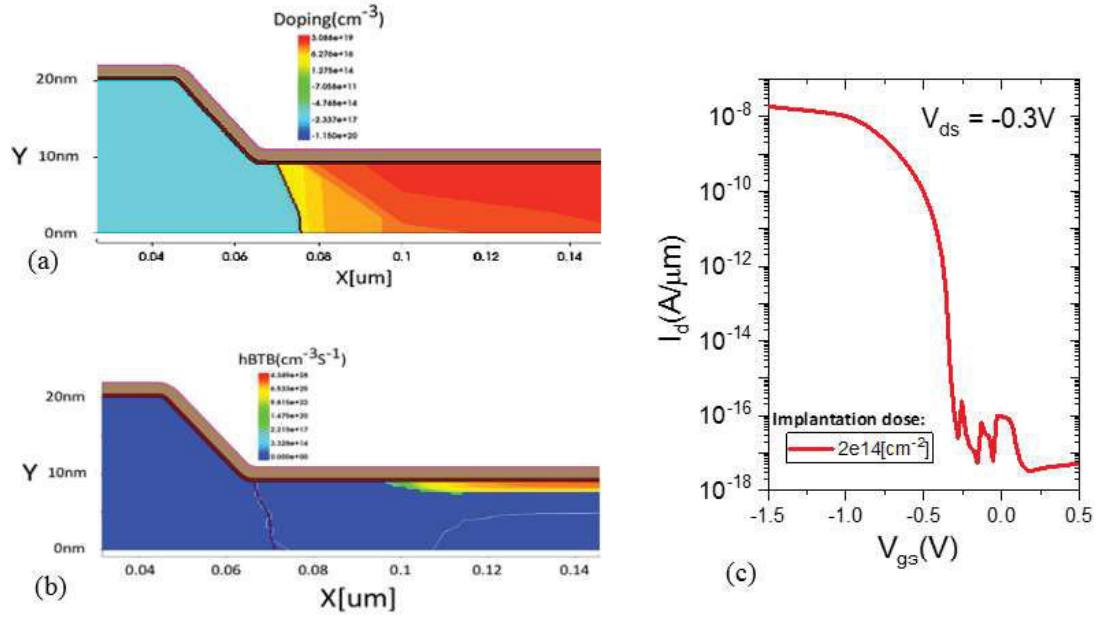
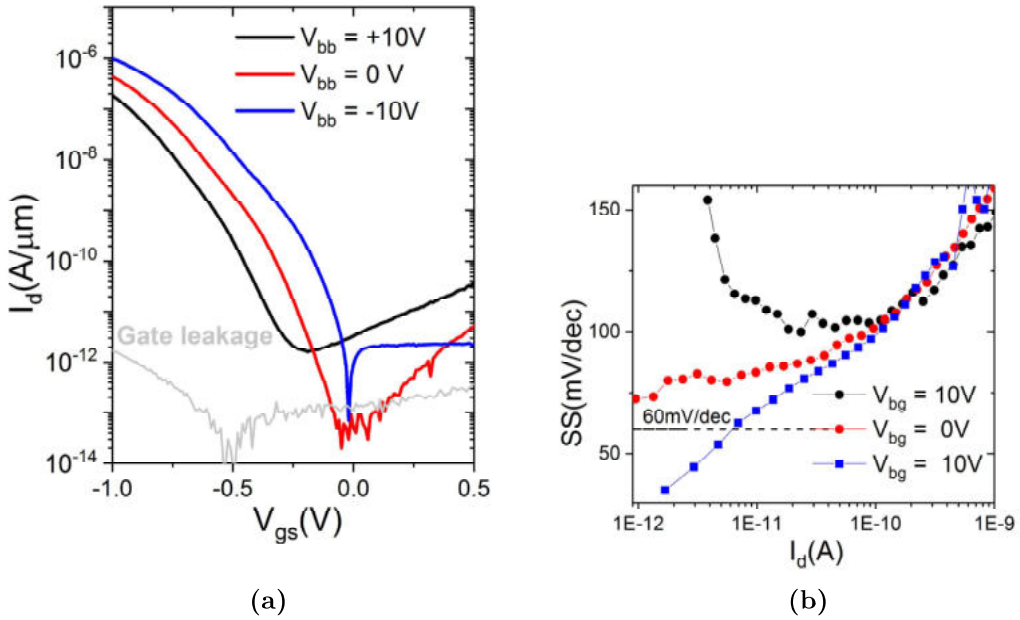


Figure 5.10: The proposed device structure with the doping only in the thin area (a). (b) simulated BTB hole generation. In contrast to the previous device doping, now BTBT only takes place under the gate on the thin area of source. (c) Simulated transfer characteristics with improved subthreshold slope.

effective band bending cannot form on the thin part. The simulated structure is shown in Figure 5.12 for a better understanding. On the other hand, a positive V_{bg} causes a stronger band-bending at the drain side. This means a higher contribution of carriers from the drain to the channel in the ambipolar behavior, leading to an increase of the ambipolar current. From these results it can be concluded that other device structures with better electrostatics such as multi and gate all around gates could further enhance the properties of the silicon line-tunneling FETs.

5.4 Analog performance

The current saturation level for analog application was measured by the output conductance , extracted from the output characteristics. As shown in Figure 5.13, g_d drops down to very small values indicating in the range of 0.01 $\frac{\mu S}{\mu m}$. This indicates very good current saturation, making the device suitable to be implemented in analog



(a) (b)

Figure 5.11: (a) DC transfer characteristics I_d-V_{gs} of transistor with doping similar to device T1. The back gate bias was set to V_{bg} = -10V, 0V, 10V. Gate leakage is shown for a reference. It is worth to note that for calculation of SS all I_d points over the noise level and gate leakage were chosen. (b) SS vs I_d plot shows the improvement in point SS by exerting negative back bias V_{bg}.

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Transconductance g_m and transconductance efficiency g_m/I_d were also extracted as shown in Figure 5.14. For our device g_m is low which is typical for planer devices. Transconductance efficiency $\frac{g_m}{I_d} = \frac{\partial I_d}{I_d \partial V_g} = \frac{ln(10)}{SS}$ as shown in Figure 5.14, g_m $/I_d$ surpasses the MOSFET limit and reaches a maximum value of 57 V^{-1}, meaning that the pTFET outperforms MOSFET in sub 60mV/dec region. However, this device is suitable for low-frequency applications as g_m values are limited and therefore cut-off frequency of the device is small.

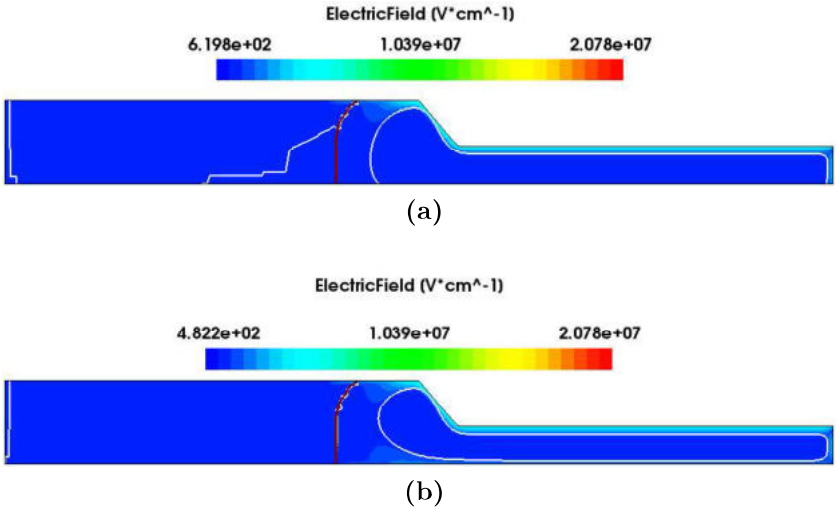


Figure 5.12: Simulated depletion regions for different back gate bias voltages (a) V_{bg} = 0 (b) V_{bg} = -10. The color range shows the electric field in the device while depletion layer is marked by the white lines. Increasing the absolute value of back gate bias extends depletion region at source and drain sides.

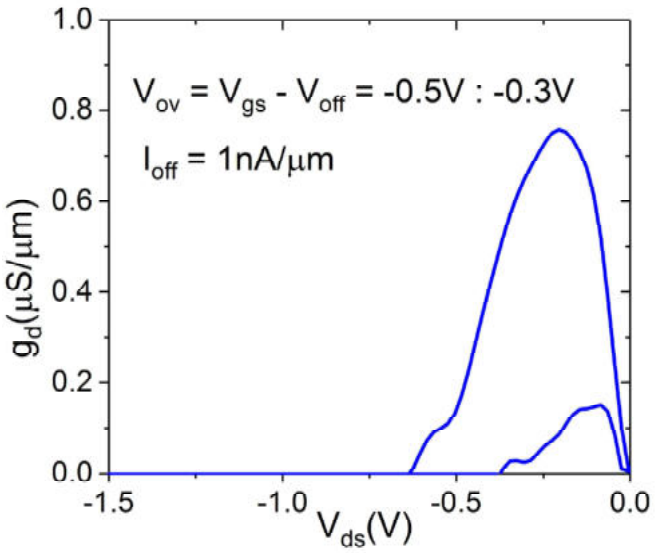


Figure 5.13: Extracted output conductance g_d from the output characteristics of device T1. g_d rapidly decreases to small values, indicating good current saturation.

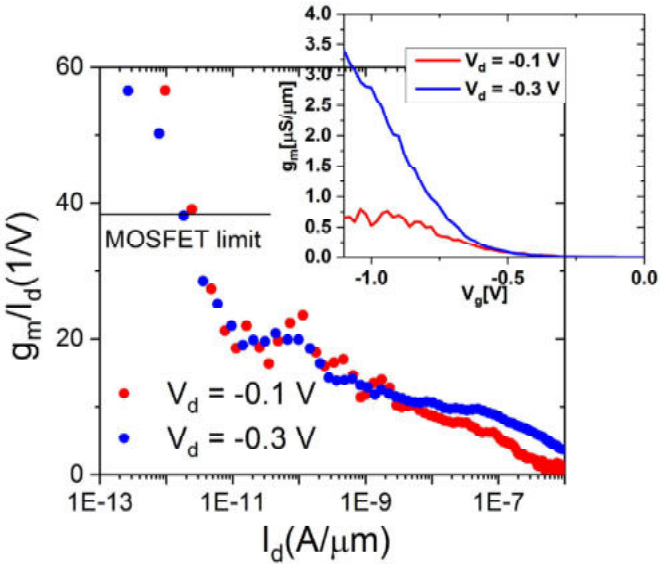
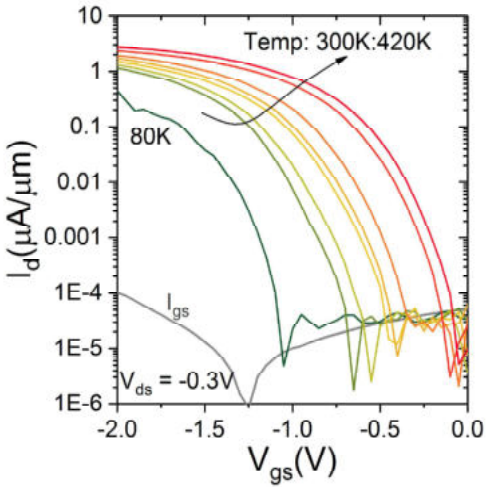


Figure 5.14: Extracted transconductance g_m and transconductance efficiency g_m/I_d for device T1. As indicated in the plot, for small currents, transconductance efficiency goes beyond values achievable by MOSFETs. Due to small g_m, this device is suitable for low-frequency applications.

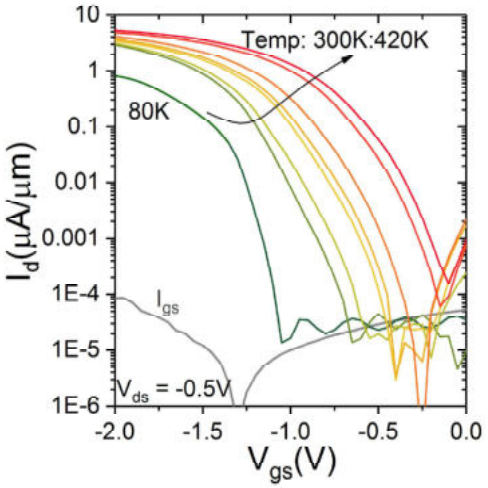
5.5 Temperature analysis

Transfer characteristics I_d - V_{gs} for a device similar to T1 at temperatures from 420K down to 300K and 80K are shown in Figure 5.15 for V_{ds} = -0.3V and V_{ds} = -0.5V. In both cases, the small change in I_{on} is observed as expected for a TFET. Moreover, it is apparent that by increasing V_{gs} the change in I_{on} current is smaller. From the curves, it seems that subthreshold slope SS does not change too much by increasing temperature. This is a good sign of reduced trap assisted tunneling effects in comparison to the NW TFET evaluated in Chapter 3. High leakage stemming from gate current and the measurement equipment have effectively masked currents below 5x10-5 $\frac{\mu S}{\mu m}$, where trap assisted tunneling would show its maximum effect on SS. Keeping this issue in mind, the minimum SS at 420K is 110mV/dec, at 300K 104mV/dec, and a 80K 85mV/dec for V_{ds} = -0.3V. These SS values were calculated for I_d above the leakage current.

To further evaluate the dependency of I_{on} current of the silicon line-tunneling FET on temperature, we will make use of the relation derived for line-tunneling normal to



(a)



(b)

Figure 5.15: Measured transfer characteristics I_d-V_{gs} for the planar line-tunneling Field at different temperatures for V_{ds} = -0.3V and V_{ds} = -0.5V.

the gate electric field lines. This is a reasonable assumption, since as it was shown in the simulations I_{on} current mainly stems from the thin part of the source where line tunneling is aligned with the electric field of gate. The relation is derived in [88] as:

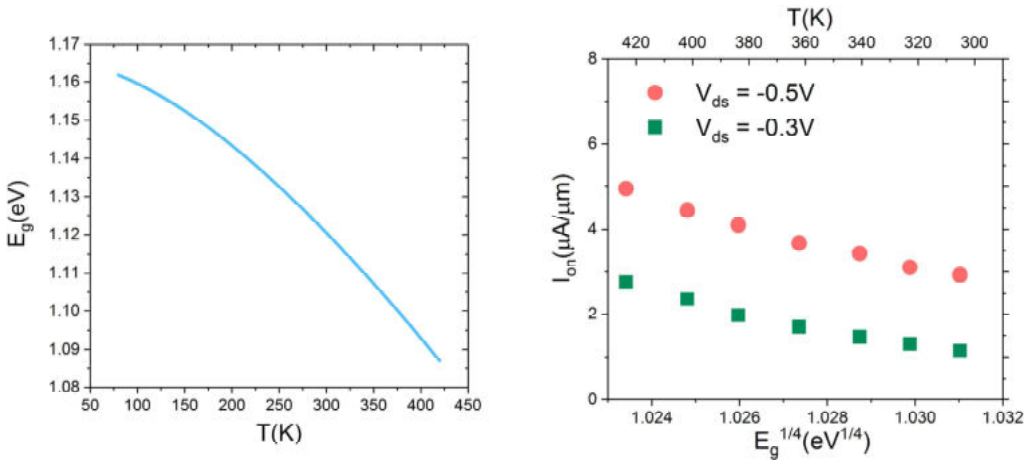
$$I_d = WLD\sqrt{V_g - V_{onset}}\exp\left\{S\sqrt{V_g - V_{onset}}\right\} \tag{5.1}$$

where V_{onset} is the required voltage to deplete the tunneling source underneath the gate, W and L are gate width and gate length. Moreover, D and S are material dependent parameters that can be found in [88, 91]. This equation is, however, derived for direct bandgap materials which in case of silicon needs some modification. This issue can be resolved by adding a multiplication parameter to the relation, derived as [92]:

$$P = (E_g n_s / 2\epsilon_s)^{1/4} \tag{5.2}$$

Now to find a relation between temperature T and I_{on} one can combine the dependency of bandgap on temperature in equation $E_g(T) = E_{g,0} - \frac{\alpha T^2}{T+\beta}$(plotted in Figure 5.16(a) for silicon) with line tunneling current relation, as shown in [92] to obtain:

$$I_d \propto {E_g}^{1/4} \tag{5.3}$$



(a) **(b)**

Figure 5.16: (a) E_g vs T temperature plot for silicon (b) I_{on} versus $E_g 1/4$ showing a linear trend with small deviation as an indication of line tunneling aligned with the gate electric field at the thin part of the source of transistor.

I_{on} versus ${E_g}^{1/4}$ has been plotted in Figure 5.16(b) for temperatures from 420K down to 300K at V_{ds} = -0.3V and V_{ds} = -0.5V. As it is apparent from the plot, there is a very good linear trend of decreasing I_{on} by increasing ${E_g}^{1/4}$, indicating presence of line-tunneling mechanism on the thin part of the source, with only slight deviation caused by approximations in the derived formula.

5.6 Conclusion

We have fabricated line-tunneling silicon pTFET with improved SS by first implantation and activation and then thinning down the source to remove EOR damages to decrease TAT. By doping via zero degree tilt implantation and high temperature annealing, we made sure that the impact of point-tunneling on current conduction would be small. Further analysis showed that, for improvement, optimization of doping and different tunneling mechanisms in the device are required. Generally, line-tunneling gives rise to a steeper slope where the electric field is stronger. In case of our device tunneling happens initially at the top corner due to fringing fields while the thinned source part of the device is the latest part where the line-tunneling starts. As a work-around we proposed an optimized doping profile to get rid of the fringing field induced tunneling and improve the device characteristics. In this new design the dopant profile under the fringing field area is essentially removed.

Chapter 6

TFET Current Mirror

This chapter deals with fabrication and characterization of silicon NW TFET current mirrors. In comparison to MOSFETs, TFETs could bring better temperature stability and lower power consumption to the analogue circuits when used with low currents[93, 94, 95]. High intrinsic voltage gain of TFET makes it also more suitable for amplifier application. It was shown by Sedighi et al[93] that TFET based operational amplifiers could achieve 5 times reduction in power dissipation and more than 10 times increase in voltage gain. Furthermore, they have shown that by using the negative differential resistance (NDR) region of TFETs, a common-source amplifier can achieve two stable operation points. NDR is anyway very hard to measure for silicon TFETs. Therefore, it does not show an immediate advantage for silicon based TFET analog circuits. Here we first explain the fabrication process of a simple two transistor current mirror, followed by characterization of high temperature behavior of the circuit.

A current mirror is generally used to keep an output current I_{out} constant at different loads. It is mainly used as an active load or current bias in analog circuits. The basic current mirror consists of two transistors, in this case two NW p-TFETs are connected as shown in Figure 6.1. Drain and gate of TFET T1 are connected to each other and it operates in the active or saturation mode. Both transistors share their gates that with this configuration I_{out} will be proportional to I_{dT1}. Moreover, drain current I_d of a TFET depends on a function comprised of drain-source V_{ds} and gate-source V_{gs} voltages. Since the drain-gate V_{gd} voltage of T1 is zero, the input current I_{in} determines the value of V_{gs}. Because both transistors share the same gate, this value of V_{gs} is also sensed by transistor T2. In the case that both transistors T1 and T2 match each other very well, by having similar electrostatics and tunneling junctions, T2 will show the same current as T1, thus imitating/mirroring the input current in the output. As discussed in Chapter 3, variability is an important issue for nanowire TFETs which makes it extremely hard to achieve a properly working

analog circuit. Depending on the biasing scheme, the circuit will either act as a current amplifier (Figure 6.1(a)) or a current bias (Figure 6.1(b)).

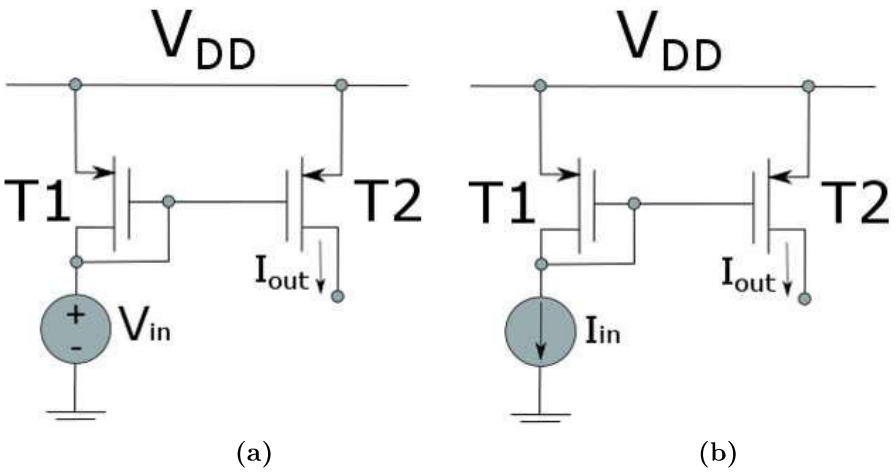


Figure 6.1: Biasing scheme of the current mirror. (a) Current amplifier. (b) Current bias

6.1 Current mirror based on silicon NW TFETs

The current mirror was fabricated on 20nm SOI wafer, apart from some minor differences, the fabrication process is similar to what was explained in Chapter 3. The TFETs were fabricated with a trigate structure. To achieve this goal, HSQ e-beam resist was replaced by PMMA resist to avoid HF to remove the resist. 3nm ALD HfO_2 and 60nm PVD TiN were deposited and patterned to act as the gate stack(Figure 6.2). As also explained in Chapter 3, in order mitigate the negative effect of TAT caused by PVD deposition of metal gate, an annealing step at 400°C in forming gas for 10 minutes was carried out. Figure 6.3 shows the biasing model of the final circuit. Both transistors share their source through a mesa which is connected to V_{DD}. Drain and gate of T1 were externally connected to each other through measurement needles. Moreover, the drain of T1 is either connected to a voltage source or a current source depending on the biasing scheme.

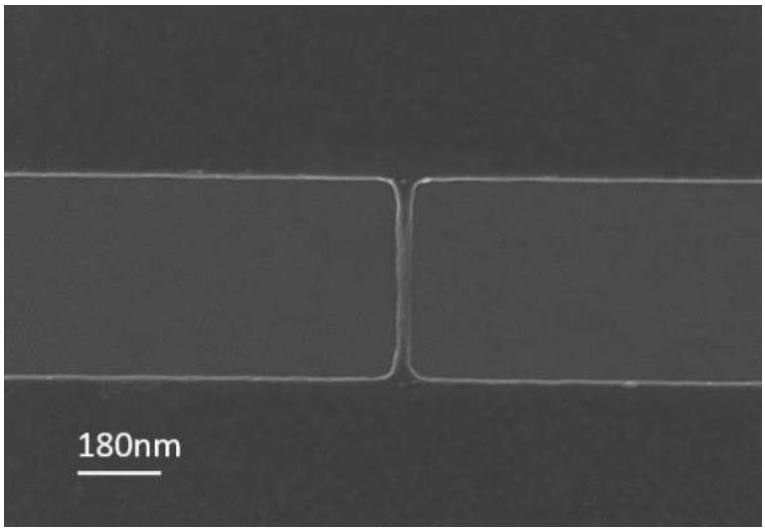


Figure 6.2: scanning electron microscopy(SEM) image of a nanowire 400nm long and 35nm wide.

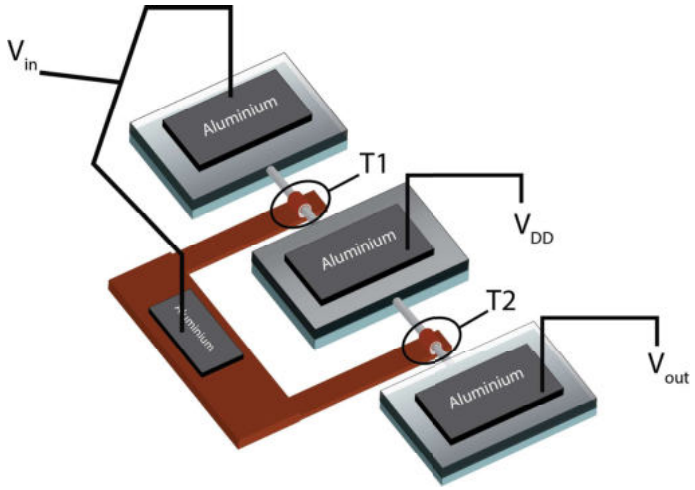


Figure 6.3: 3D schematic of the fabricated current mirror circuit with biasing voltage layout.

6.1.1 DC and high temperature characterization of the current mirror

The current mirror was biased at different V_{in} voltages in order to record I_{out} and its relation to I_{T1} at different voltages. The output characteristics of T2 (I_{out}- V_{out}) at room temperature are shown in Figure 6.4(a), where the value of I_{T1} for each case

is written on top of the curve. As visible, the T2 shows good saturation and some super-linear onset. Moreover, it also mirrors the I_{T1} current pretty well. Although the mirroring is not perfect, which is due to non-ideal match between T1 and T2 due to process variations. Since the circuit is being biased in current amplifier mode, as an important figure of merit the mirror ratio(I_{out}/ I_{in}) is depicted at room temperature at V_{DD} = 0.5V, and shown in Figure 6.4(b). The mirror ratio changes around value of 1 and decreases by increasing V_{in}. This is related to different behavior of the transistors at different voltages due to device variations.

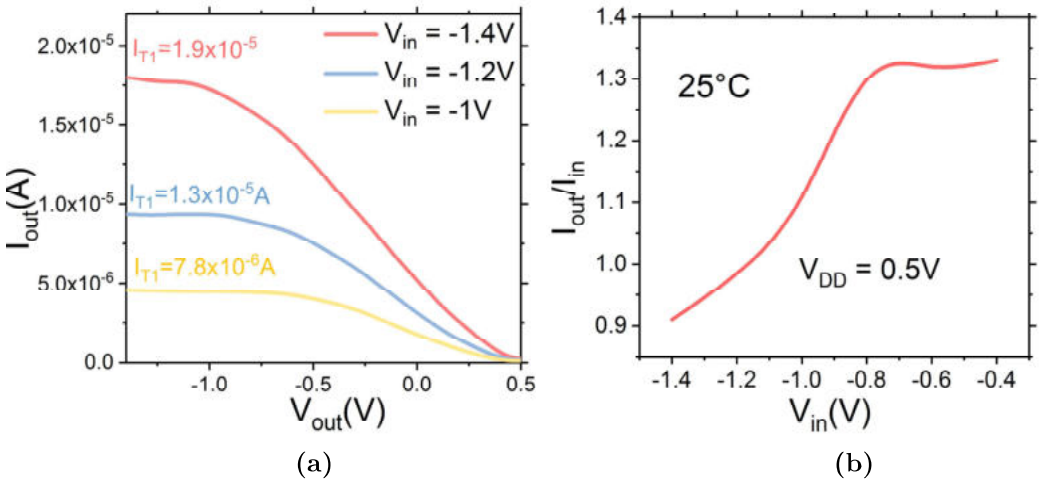
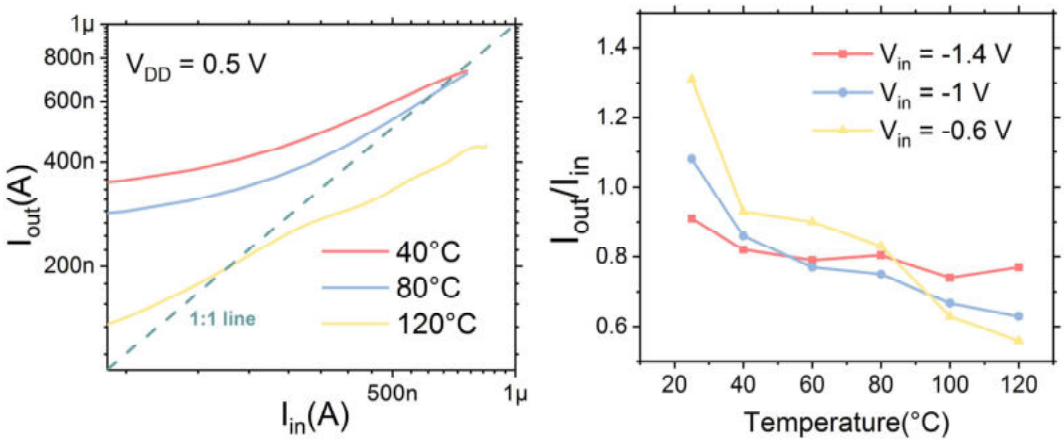


Figure 6.4: (a) I_{out} current versus V_{out} voltage at different V_{in} voltages based on biasing scheme in Figure 6.1(a) showing good saturation and match between transistors. (b) Mirror ratio I_{out}/I_{in} is plotted vs V_{in} as a figure of merit for the current amplifier biasing scheme at a fixed V_{DD} = 0.5V.

In order to observe the temperature dependence of the fabricated current mirror, the circuit was heated up to 120°C and measured at both bias configuration shown in Figure 6.5. I_{out} vs I_{in} plot for different temperatures is shown at Figure 6.5(a). I_{in} was swept from 1x10^{-7}A to 1x10^{-6}A while I_{out} was measured in the saturation region of T2 and V_{DD} was fixed at 0.5V. The dashed line depicts the 1:1 ratio as a reference. The mirror ratio (MR) is larger than 1 at small I_{in}, and decreases with I_{in}. As temperature increases, I_{out} decreases at the same I_{in}, which is caused by the different temperature T dependence of T1 and T2.

The MR as a function of temperature is displayed in Figure 6.5(b). The MR

value decreases with increasing temperature. At higher absolute V_{in} the MR value is more stable with temperature. This is because at higher gate voltage band to band tunneling, which is less temperature dependent, is dominant. At lower gate voltage trap assisted tunneling has a larger contribution, resulting in higher temperature dependence. Therefore, suppressing TAT is also a key challenge for higher temperature applications of TFET analog circuits.



(a) (b)

Figure 6.5: (a) Measured I_{out} of the current mirror by changing I_{in} for biasing scheme in Figure 6.1(b). The plot reveals reduction of I_{out} for increasing T at constant I_{in}. (b) Mirror ratio I_{out}/I_{in} for three different V_{in} voltages based on biasing scheme of Figure 6.1(a). The I_{T1} at 25°C is also written for each plot.

6.1.2 Temperature sensitivity of the individual transistors

In order to explain the temperature dependence of the current mirror in more detail, we have conducted high temperature measurement on each individual device of the circuit. Transfer characteristics I_d-V_{gs} for each device were measured from 25°C to 140°C as shown in Figure 6.6. Both device characteristics are very similar to each other in terms of slope, onset voltage and on-current, which is very important for the function of analog circuits. Transistor T1 has an average SS of 106mV/dec and transistor T2 achieves an average SS of 107mV/dec over three orders of magnitude at room temperature, showing very close behavior. In order to make an in depth,

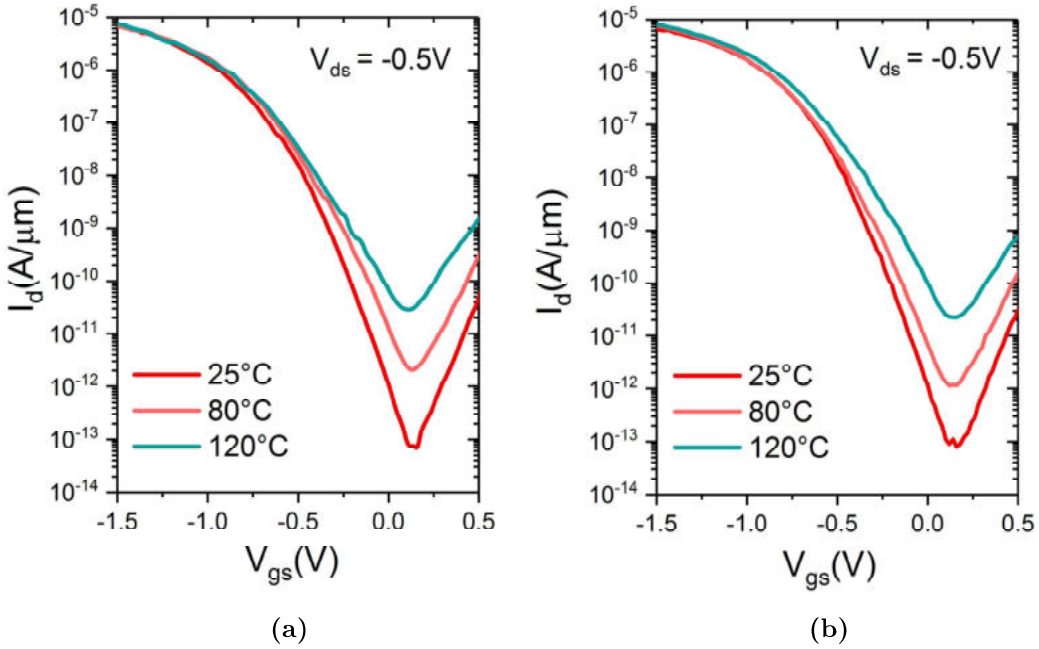
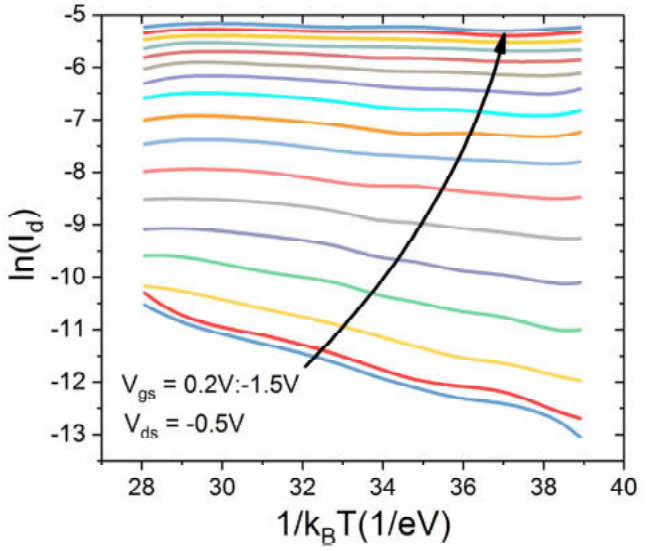


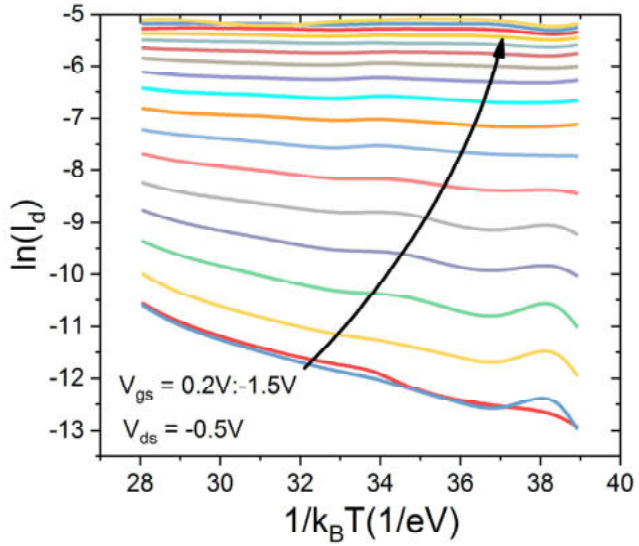
Figure 6.6: Transfer characteristics I_d-V_{gs} for each device measured from 25°C to 120°C . (a) T1 transistor (b) T2 transistor

we measured the activation energy for each transistor. As shown in chapter 3,an Arrhenius plot can be plotted by taking the natural logarithm of I_d against $\frac{1}{K_B T}$. It was displayed for V_{gs} = 0.2V to -1.5V at V_d = -0.5V as shown in Figure 6.7. The slope of each line, corresponding to a specific V_{gs}, is the activation energy E_a at that particular V_{gs}. The activation energy is basically a measure of current sensitivity to temperature. In other words, when E_a is larger, current varies more strongly by changing temperature.

The resulting activation energy E_a plot is shown at Figure 6.8 for both T1 and T2 transistor calculated at V_{ds} = -0.5V. T1 tends always to have higher E_a than T2 especially at smaller V_{gs} voltages, explaining the MR dependence of V_{in} shown in Figure 6.5(b). Basically when the circuit is supplied by a certain input current I_{ref}, as temperature increases, V_{gs} of T1 will change to match itself to the new conditions. At a higher temperature, T1 can achieve the same I_{ref} at a lower V_{gs} which translates into a lower V_{gs} for T2. As T2 does not change as strongly as T1 with temperature,



(a)



(b)

Figure 6.7: Arrhenius plot of T1 and T2 for different V_{gs} voltages from 0.2V to -1.5V at V_{ds} = -0.5V. The slope of each line represents the activation energy Ea, which basically shows the sensitivity of the current to temperature changes at a specific voltage.

there will be less current flowing through it. This process leads to a decrease in the mirror ratio.

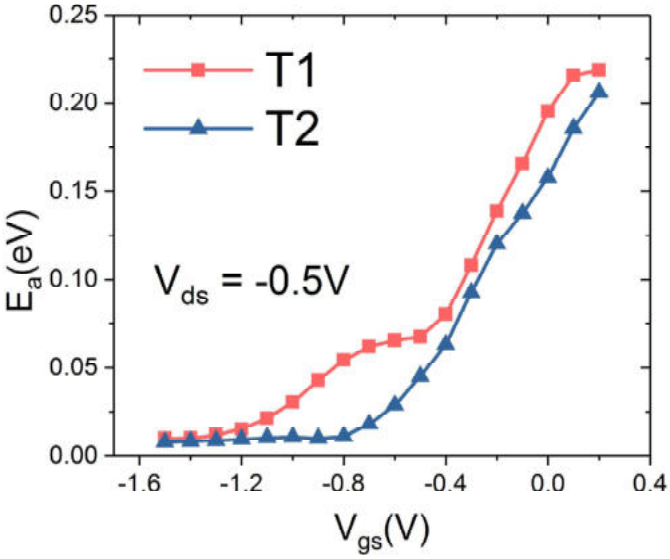


Figure 6.8: Activation energy Ea plot for both transistors T1 and T2 of the current mirror as a function of gate voltage V_{gs}. The plot shows higher sensitivity of T1 transistor current to temperature with respect to transistor T2.

Lastly, the experimental results have been compared to the CM simulation carried out by A.Biswas et al [96]. Based on the simulations, MR is affected by increasing temperature and for a stable operation at elevated temperatures, CM needs to be operated at higher biases. This is in agreement with our results on temperature stability of the fabricated TFET CM. However, I_{out} in simulations does not change significantly with temperature T at a specific I_{in} for higher currents which differs from our finding of Figure 6.4(a). This is due to the fact that the TFETs in the simulation are completely matched and have exactly the same characteristics.

6.2 Conclusion

Current mirrors based on silicon NW TFETs proved to have very good temperature stability at higher temperatures when both transistors are in the band to band tunneling regime. These results further indicated the importance of matching TFETs for analog applications. Even though the characteristics of transistors may be very similar at room temperature, their drain current I_d temperature sensitivity may be

different. For a real MOSFET analog application, mismatch between neighboring transistors can be controlled by increasing their area[97]. In TFET based analogue circuits, the biggest obstacle to achieve temperature stability is suppression of TAT. TAT results in thermionic conduction which is highly dependent on temperature. Since TAT dominates at lower voltages, the circuit had to be biased with high voltage to achieve temperature stability which is in contrast to the goal of achieving low-power circuits. So in order to really benefit from the temperature stability of TFETs at low voltages, new methods of fabrication and layer deposition should be employed to reduce TAT caused by interface and defect traps.

Chapter 7

Conclusion and outlook

Within the scheme of this work, we investigated various designs of silicon based TFETs to enhance the on-current I_{on}, decrease impact of TAT and suppress ambipolarity. Our approach to address on-current was established on basic design rules derived from the theoretical BTBT probability expressions to decrease the screening length λ by scaling the device and gate structure and optimizing E_g and m^* by employing strained silicon wafers. Highly scaled single nanowire TFETs with high-k dielectric were fabricated to achieve the optimum electrostatic control of the channel by minimizing λ_{chan}. Furthermore the use of single nanowire devices as opposed to arrays of NWs due to the exponential susceptibility of BTBT probability to process variations among the nanowires of an array. To minimize λ_{dop}, key process parameters, specifically implantation and activation, were carefully adjusted in different settings. The highlight of the results was demonstration of an optimized single NW GAA TFET with NW dimensions of 10nm x 40nm and record on-current $I_{on} = 15\mu A/\mu m$ at a supply voltage V_{dd}= 0.5V with average slope of SS_{avg} = 74mV/dec over four orders of drain current I_d.

Further evaluation of the fabricated nanowires devices by means of low-temperature measurements proved that an important limiting factor in achieving sub-60mV/de average switching slopes is a result of carrier conduction by means of trap assisted tunneling(TAT) at low voltages. The high significance of TAT stems from the interface traps and also correlated to the damage in silicon caused by ion implantation which are not annealed by the low temperature dopant activation. Charge pumping measurements were carried out to quantify density of interface traps D_{it} for the nanowires. They indicated that deposition of the gate metal by means of PVD inflated number of interface traps. However, it was demonstrated that these traps can be decreased significantly via forming gas annealing. Nevertheless, the measured D_{it} was about one order of magnitude higher than the optimum value, and thus led to

degrading SS by screening gate control.

In addition, the parasitic ambipolar behavior which is inherent to the TFET operation was systematically suppressed. Simulations predicted that a gate-drain underlap would effectively worsen the drain junction and decrease the ambipolar behavior, depending on the length of the underlap. In experiments, we employed a SiO_2 spacer to separate the drain silicide and the channel forming the purported underlap. Measurements of the fabricated n- and p- TFETs exhibited that the ambipolar behavior of these devices vanished completely, making them ideal for circuit applications.

To achieve better subthreshold performance, novel silicon tunnel FETs based on line-tunneling are designed and fabricated. The fabricated devices show on-current of Ion=2.55×10^{-7}A/μm at V_{ds}=V_{on}=$V_{gs}-V_{off}$=$-$0.5V for an I_{off}=1nA/μmand an average SS of 55mV/dec over two orders of magnitude of drain current Id. We achieved this by first implantation and high temperature activation of dopants and then thinning down the source to remove end-of-range(EOR) damage. This is important to decrease negative effect of TAT. Further analysis by support of simulations show that line-tunneling happens initially at the top corner due to fringing fields while the thinned source part of the device is the latest part where the tunneling starts, therefore doping optimization to control different tunneling mechanisms in the device is mandatory.

Feasibility of TFETs for digital and analog circuits was also evaluated. Complementary FET inverters have been fabricated and characterized based on the single NW TFETs on the same mesa with and without ambipolar behavior. In case of the inverters with ambipolarity, it was shown that the ambipolar behavior degrades the voltage transfer characteristics by preventing the logical levels to match the actual bias levels. Nevertheless, the inverter achieves sufficient voltage gain down to V_{dd} = 0.8V. High-temperature measurement on the inverter revealed that the inverter can maintain its function for high bias points where it is less susceptible to nonlinear behavior in output characteristics caused by temperature dependent processes like TAT. Inverters based on TFETs with suppressed ambipolar behavior exhibited greatly improved noise margins where the logic levels matched the actual bias points. However, due to on-set voltage separation between n- and p-TFETs, higher bias points were needed for proper operation of the devices.

Feasibility of TFETs for high temperature stability of analogue circuits was also investigated. A two-transistor current mirror was fabricated by employing matched

p-TFETs on the same mesa. Circuit characterization along high-temperature measurements up to 120°C revealed stable operation of the current mirror for certain range of voltages. Further evaluation of temperature behavior of each individual TFET through activation energy Ea measurements showed that the stable circuit operation is brought about when the transistors function deep in the BTBT region.

For future work, to make these devices feasible for practical applications, further improvements are mandatory. Better electrostatics to improve BTBT could be achieved by improving EOT through dielectrics with higher-k and preventing formation of interfacial SiO_2 layer. Moreover, smaller band-gap materials instead of silicon are beneficial for increasing BTBT. Unfortunately, any attempt to improve BTBT also amplifies TAT, the most challenging issue to be tackled. Optimized surface cleaning and dielectric deposition techniques are needed to reduce D_{it} by at least one order of magnitude. With novel device structures, like the line-tunneling silicon TFETs presented in this work subthreshold slopes even below 60 mV/dec could be achieved. Nevertheless, our devices can be further optimized by removing dopant concentration below the fringing fields. This is achievable by optimum implantation and source thinning processes. By optimizing single devices, TFET based circuits will enjoy enhanced high temperature stability at even lower operating voltages.

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